Training Manual

LG TRAINING CENTER

50PV450 Plasma Display

TruSlim FRAME

600Hz Sub Field Driving

Advanced Single Scan Troubleshooting
50" Class Full HD 1080p Plasma TV
(49.9" diagonally)

LG Life's Good

Published May 13th, 2011

Overview of Topics to be Discussed

Preliminary:
Contact Information, Preliminary Matters, Specifications,
Plasma Overview, General Troubleshooting Steps,
Disassembly Instructions, Voltage and Signal Distribution

Troubleshooting:
Circuit Board Operation, Troubleshooting and Alignment of :

- Switch Mode Power Supply No "VS On" command input to SMPS from the Main Board.
- Y-SUS Board
- Y-Drive Boards (1 Upper and 1 Lower).
- Z-SUS Board Uses a Z-SUB Board for panel drive connection.
- Control Board
- X Drive Boards (3) Drives 15 TCPs (5 per/board). Each TCP drives 384 vertical electrodes.
- Main Board:
- Front IR/Intelligent Sensor
- Interconnect Diagram: 11X17 Foldout Section used as a quick reference sheet.

50PV450 Plasma Display

Section 1

This Section will cover Contact Information and remind the Technician of Important Safety Precautions for the Customer's Safety as well as the Technician's and the Equipment.

Basic Troubleshooting Techniques which can save time and money sometimes can be overlooked. These techniques will also be presented.

This Section will get the Technician familiar with the Disassembly, Identification and Layout of the Plasma Display Panel.

At the end of this Section the Technician should be able to Identify the Circuit Boards and have the ability and knowledge necessary to safely remove and replace any Circuit Board or Assembly.

LG Contact Information

Customer Service (and Part Sales)	**(800) 243-0000**
Technical Support (and Part Sales)	**(800) 847-7597**
USA Website (GSFS)	**http://gsfs-america.lge.com**
Customer Service Website	**http://www.us.lgservice.com**
Knowledgebase Website	**http://lgtechassist.com** ← New: 2010 Models Wireless Ready Software Downloads
LG Web Training	**https://lge.webex.com** ← Presentations with Audio/Video and Screen Marks
LG CS Learning Academy	**http://ln.lge.com/ilearn** ← **http://136.166.4.200**

Training Manuals, Schematics with Navigational Bookmarks, Start-Up Sequence, Owner's Guides, Interconnect Diagrams, Dimensions, Connector IDs, Product Pictures and Features.

Also available on the Plasma Page:
PDP Panel Alignment Handbook,
Plasma Control Board ROM Update (Jig required)

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LG Electronics Alabama, Inc.
201 James Record Road, Huntsville, AL, 35813.

IMPORTANT SAFETY NOTICE

The information in this training manual is intended for use by persons possessing an adequate background in electrical equipment, electronic devices, and mechanical systems. In any attempt to repair a major Product, personal injury and property damage can result. The manufacturer or seller maintains no liability for the interpretation of this information, nor can it assume any liability in conjunction with its use. When servicing this product, under no circumstances should the original design be modified or altered without permission from LG Electronics. Unauthorized modifications will not only void the warranty, but may lead to property damage or user injury.
If wires, screws, clips, straps, nuts, or washers used to complete a ground path are removed for service, they must be returned to their original positions and properly fastened.

CAUTION

To avoid personal injury, disconnect the power before servicing this product. If electrical power is required for diagnosis or test purposes, disconnect the power immediately after performing the necessary checks. Also be aware that many household products present a weight hazard.
At least two people should be involved in the installation or servicing of such devices.
Failure to consider the weight of an product could result in physical injury.

Preliminary Matters (The Fine Print)

ESD Notice (Electrostatic Static Discharge)

Today's sophisticated electronics are electrostatic discharge (ESD) sensitive. ESD can weaken or damage the electronics in a manner that renders them inoperative or reduces the time until their next failure. Connect an ESD wrist strap to a ground connection point or unpainted metal in the product. Alternatively, you can touch your finger repeatedly to a ground connection point or unpainted metal in the product. Before removing a replacement part from its package, touch the anti-static bag to a ground connection point or unpainted metal in the product. Handle the electronic control assembly by its edges only. When repackaging a failed electronic device in an anti-static bag, observe these same precautions.

Regulatory Information

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses, and can radiate radio frequency energy, and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: Reorient or relocate the receiving antenna; Increase the separation between the equipment and the receiver; Connect the equipment to an outlet on a different circuit than that to which the receiver is connected; or consult the dealer or an experienced radio/TV technician for help.

Safety and Handling, Checking Points

Safety & Handling Regulations

1. Approximately 10 minute pre-run time is required before any adjustments are performed.
2. Refer to the silk screening on the Switch Mode Power Supply for proper Voltage and Current listings and manufacturer's cautions.
3. Refer to the Voltage Sticker on the Panel when making adjustments on the Power Supply, Y-SUS and Z-SUS Boards.
4. Always adjust to the specified voltage level (+/- ½ volt) unless otherwise specified.
5. Be cautious of electric shock from the PDP module since the PDP module uses high voltage, check that the Power Supply and Drive Circuits are completely discharged because of residual current stored before Circuit Board removal.
5. C-MOS circuits are used extensively for processing the Drive Signals and should be protected from static electricity.
6. The PDP Module must be carried by two people. **Always carry vertical NOT horizontal.**
7. **The Plasma television should be transported vertically NOT horizontally.**
8. Exercise care when making voltage and waveform checks to prevent costly short circuits from damaging the unit.
9. Be cautious of lost screws and other metal objects to prevent a possible short in the circuitry.
10. **New Plasma Models have thinner Display Panels and Frames than previous models. Be careful when lifting Plasma Display's because flexing the panel may damage the frame mounts or panel.**

Checking Points to be Considered

1. Check the appearance of the Replacement Panel and Circuit Boards for both physical damage and part number accuracy.
2. Check the model label. Verify model names and board model matches.
3. Check details of defective condition and history. Example: Y-SUS or Y-Drive Board Failure, Mal-discharge on screen, etc.

Define, Localize, Isolate and Correct

•**Define** Look at the symptom carefully and determine what circuits could be causing the failure. Use your senses Sight, Smell, Touch and Hearing. Look for burned parts and check for possible overheated components. Capacitors will sometimes leak dielectric material and give off a distinct odor. Listen for frequency changes which may occur with a Power Supply load failure, listen for the "click" of a relay closing, remember to observe the Front Power Indicator LED, if lit, it is a quick indication of Standby Voltage.

•**Localize** After carefully checking the symptom and determining the circuits to be checked and after giving a thorough examination using your senses the first check should always be the DC Supply Voltages to those circuits under test. Always confirm the supplies are not only the proper level but be sure they are noise free. If the supplies are missing check the resistance for possible short circuits.

•**Isolate** To further isolate the failure, check for the proper waveforms with the Oscilloscope to make a final determination of the failure. Look for correct Amplitude Phasing and Timing of the signals also check for the proper Duty Cycle of the signals. Sometimes "glitches" or "road bumps" will be an indication of an imminent failure.

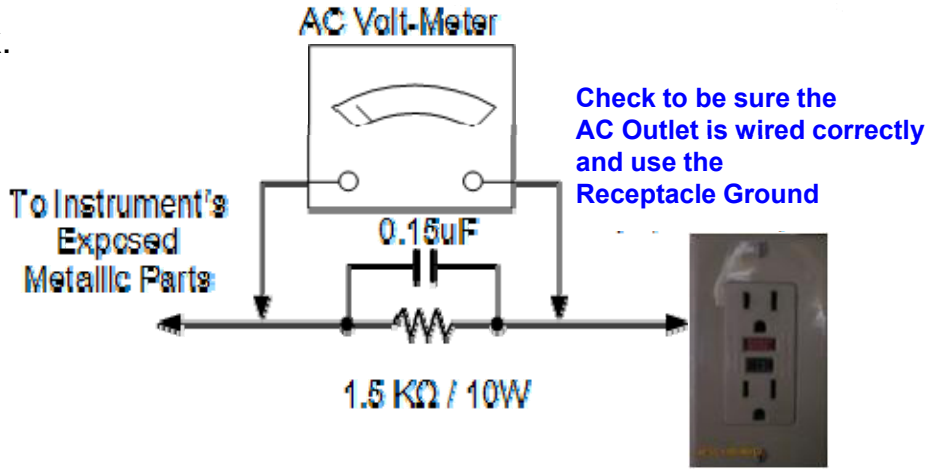
•**Correct** The final step is to correct the problem. Be careful of ESD and make sure to check the DC Supplies for proper levels. Make all necessary adjustments and lastly always perform a **Safety AC Leakage Test** before returning the product back to the Customer.

AC Leakage Test Procedure

Leakage Current Cold Check (Antenna Cold Check)
With the instrument AC plug removed from an AC source, connect an electrical jumper across the two AC plug prongs. Connect one lead of an ohm-meter to the AC plug prongs tied together and touch the other lead one at a time to any exposed metallic part on the set. Such as the antenna terminal, LAN jack, AV connections, HDMI input shield, PC input shield, etc.
If the exposed metallic part has a return path to the chassis,
the measurement resistance should be between 1MΩ and 5.2MΩ.
When the exposed metal has no return path to the chassis, the reading must be infinite.
If an abnormality exists it must be corrected before the receiver is returned to the customer.

Leakage Current Hot Check (See figure)
Plug the AC cord directly into the AC outlet.

Do not use a line isolation transformer during this check.
Connect 1.5K/10watt resistor in parallel with a 0.15uF capacitor between a known good earth ground (Water Pipe, Conduit, etc.) and the exposed metallic parts.
Measure the AC voltage across the resistor using AC voltmeter with 1000 ohms/volt or more sensitivity.
Any voltage measured must not exceed 0.75 volt RMS which corresponds to 0.5mA.
In case any measurement is out of the limits specified, there is possibility of shock hazard and the set must be checked and repaired before it is returned to the customer.



50PV450 PRODUCT INFORMATION SECTION

This section of the manual will discuss the specifications of the 50PV450 Advanced Single Scan Plasma Display Television.

1080P PLASMA HDTV

50" Class (49.9" diagonal)

For Full Specifications
See the Specification Sheet

- **TruSlim Frame**
- **600Hz Max Sub Field Driving**
- **Full HD 1080p Resolution**
- **ENERGY STAR® Qualified**
- **Picture Wizard II**
- **Intelligent Sensor**
- **Smart Energy Saving**
- **ISFccc® Ready**

50PV450 Logo Familiarization

FULL HD RESOLUTION 1080P HD Resolution Pixels: 1920 (H) × 1080 (V)
Enjoy twice the picture quality of standard HDTV with almost double the pixel resolution. See sharper details like never before. Just imagine a Blu-ray disc or video game seen on your new LG Full HD 1080p TV.

Clear Voice Clearer dialogue sound
Automatically enhances and amplifies the sound of the human voice frequency range to provide high-quality dialogue when background noise swells.

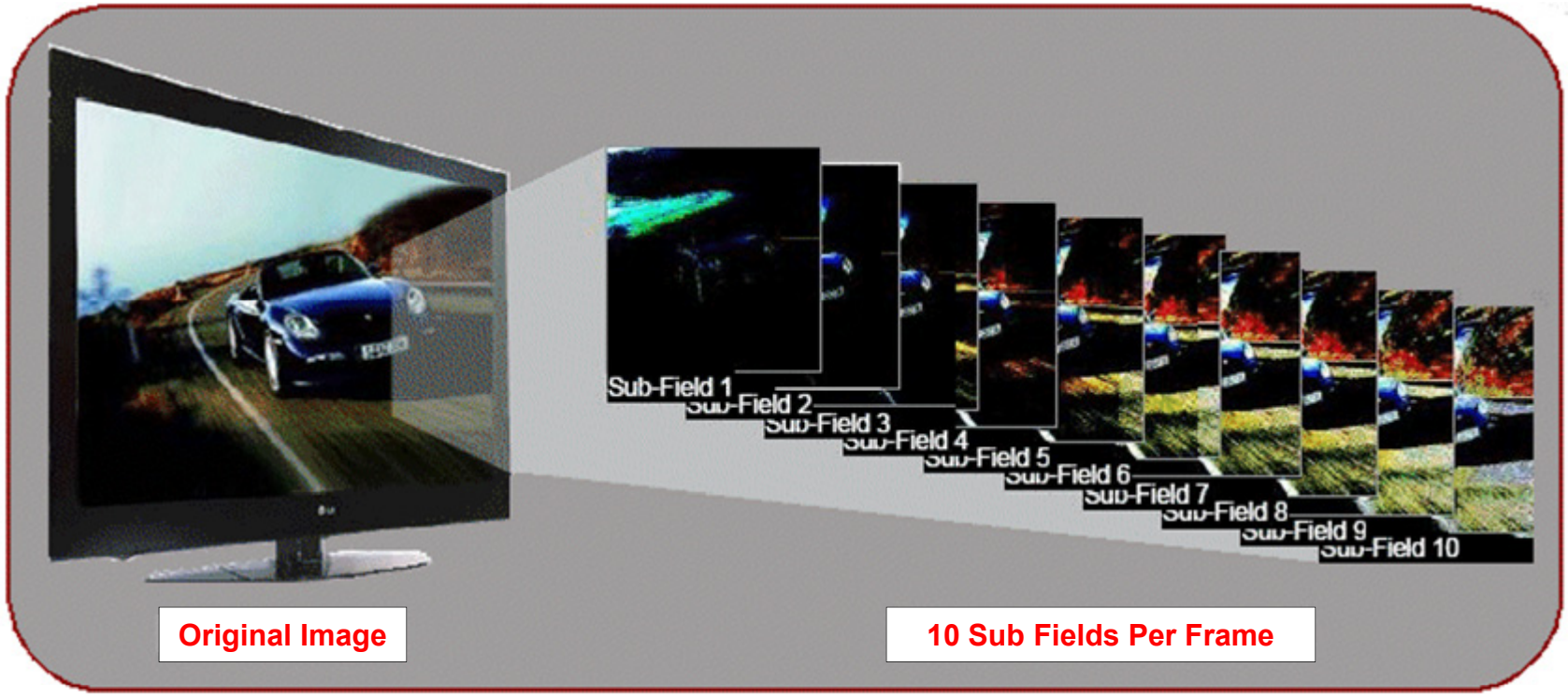
Save Energy, Save Money
It reduces the plasma display's power consumption.
The default factory setting complies with the Energy Star requirements and is adjusted to the comfortable level to be viewed at home.
(Turns on Intelligent Sensor).

Save Energy, Save Money
Home electronic products use energy when they're off to power features like clock displays and remote controls. Those that have earned the ENERGY STAR use as much as 60% less energy to perform these functions, while providing the same performance at the same price as less-efficient models. Less energy means you pay less on your energy bill. Draws less than 1 Watt in stand by.

(600 Hz Sub Field Driving)

- **600 Hz Sub Field Driving is achieved by using 10 sub-fields per frame process (vs. Comp. 8 sub-field/frame)**

- **No smeared images during fast motion scenes**



Sub Field firing occurs using wall charge and polarity differences between Y-SUS and Z-SUS signals.

50PV450 Remote Control

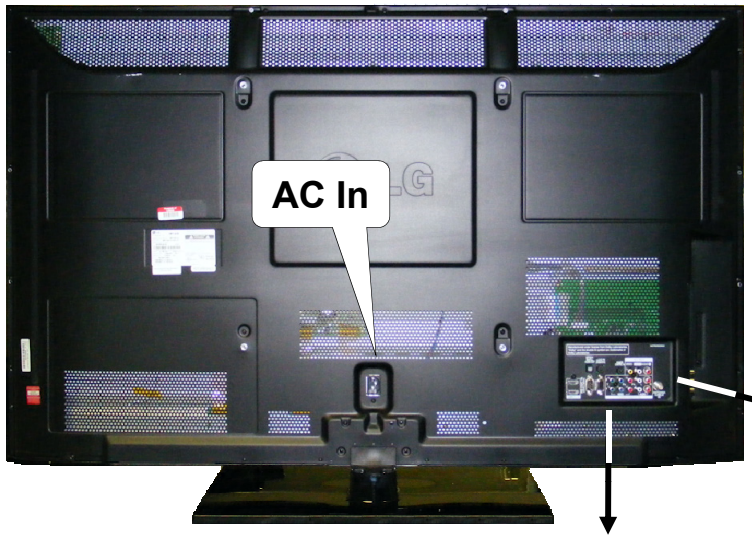
p/n AKB72914053

TOP PORTION

BOTTOM PORTION

50PV450 Rear and Side Input Jacks

USB port for Software Upgrades,
Music, Videos and Photos



SIDE INPUTS

USB

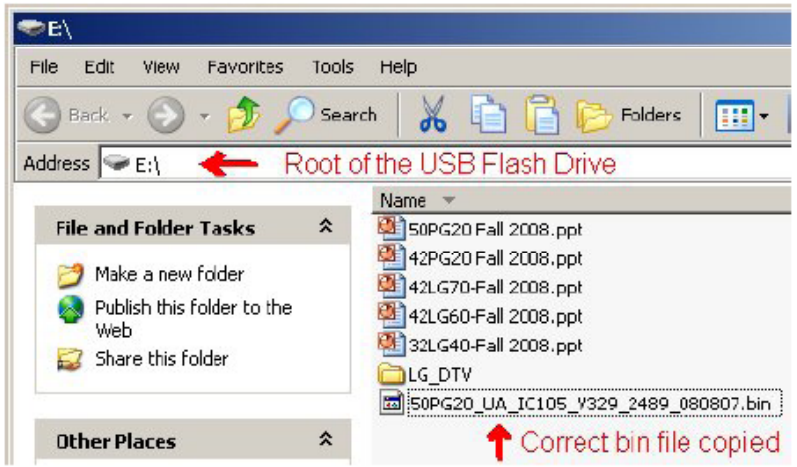
HDMI 3

Composite Video/Audio

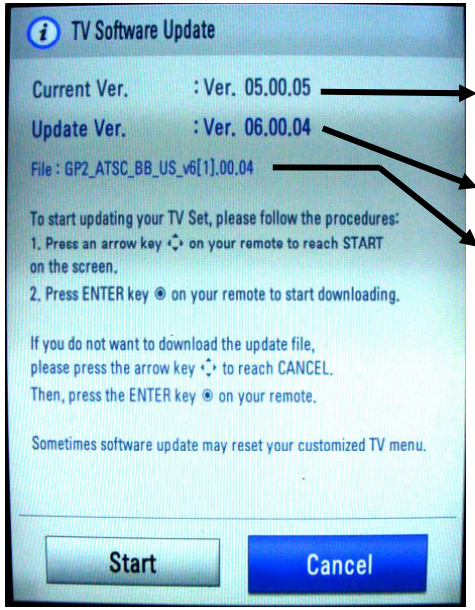
REAR INPUTS

Generic Plasma USB Automatic Software Download Instructions

1) Download the Software File.



2) Copy new software (xxx.bin) into the root of the Jump Drive. Make sure you have the correct software file.
3) With TV turned on, insert USB flash drive.
4) You can see the message
"TV Software Upgrade" (See figure on right)
5) Cursor left and highlight "START" Button and push "Enter" button using the remote control.
6) You can see the download progress Bar.
7) Do not unplug until unit has automatically restarted.
8) When download is completed, you will see "COMPLETE".
9) Your TV will be restarted automatically.



Currently Installed Version

Software Version found on the USB Flash Drive

File found on the USB Flash Drive

Highlight Start Press Select

*** CAUTION:**
Do not remove AC power or the USB Flash Drive.
Do not turn off Power, during the upgrade process.

Software Files are now available from LGTechassist.com

Manual Software Download:

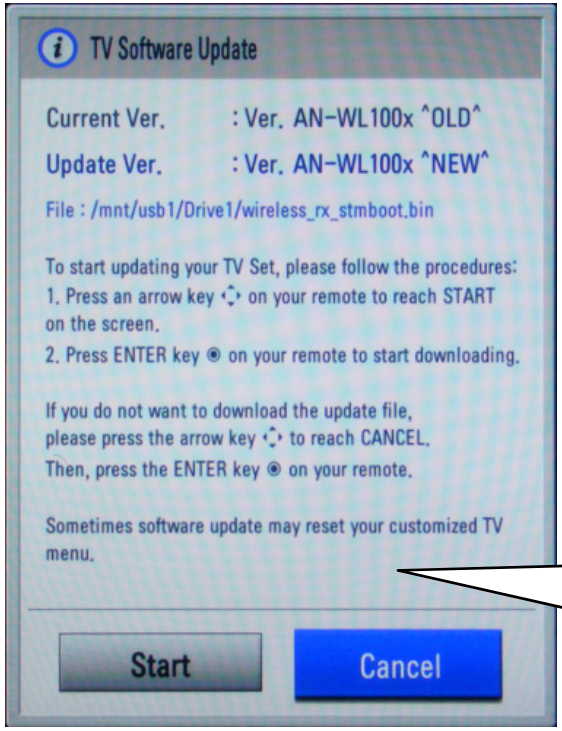
Prepare the Jump Drive as described in the “USB Automatic Download” section and insert it into the USB port.
Bring up the Customer’s Menu and scroll to “OPTIONS”, (Nothing should be highlighted on the right side).
Press the “FAV” key 7 times to bring up the first screen for Manual Download Screen (Expert Mode).

1

2 Scroll down and highlight “Options”

Press the “FAV” key 7 times

3



Location of files found On the Jump Drive

4 Highlight the Software update file the highlight “Start” and press “SELECT” to begin the download process.

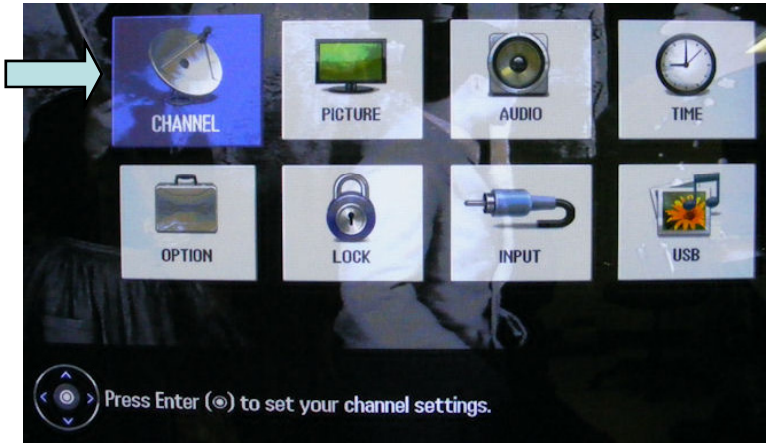
WARNING:
Use extreme Caution when using the Manual “Forced” Download Menu. Any file can be downloaded when selected and may cause the Main board to become inoperative if the incorrect file was selected.

Accessing the Host Diagnostic Screen

Use the Host Diagnostic screen to investigate the signal quality of a problem channel.

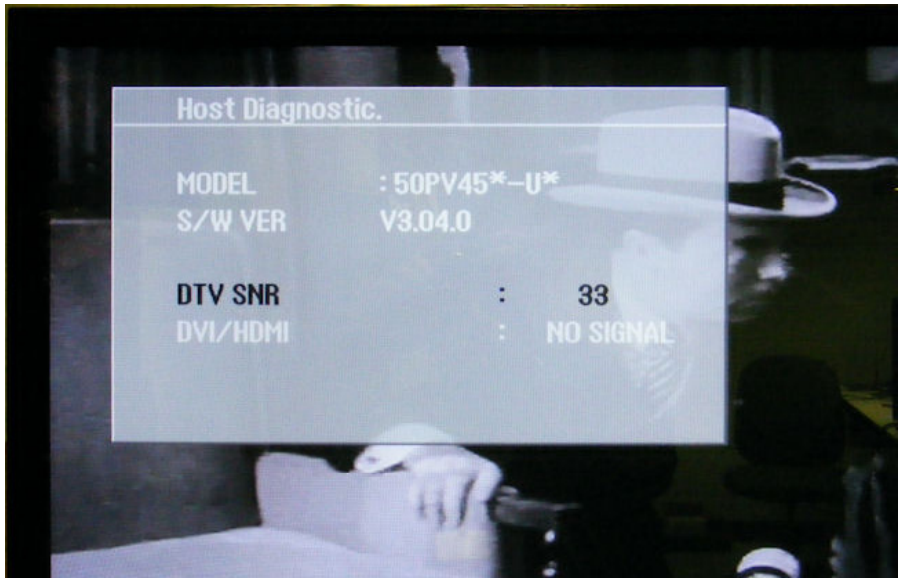
1) Place Television on the digital channel that may be showing problems.

2) Bring up the Customer's Menu. Highlight "**CHANNEL**". Press "**ENTER**" on the remote.



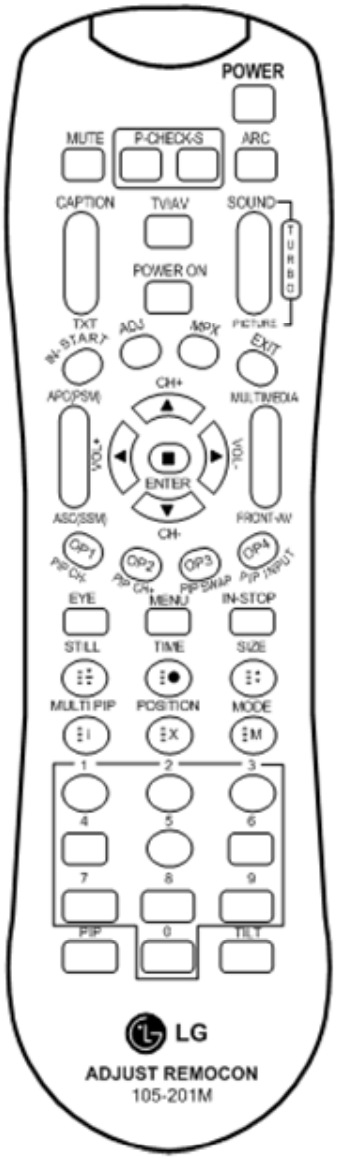
3) The "CHANNEL" Menu appears.

4) Press the (1) Key 5 to 8 times.
The Host Diagnostics screen appears.



DTV SNR: Digital Television Signal to Noise Ratio
Over the Air: 8VSB (Above 20 is good)
Cable Digital: QAM 64 (Above 24 is good)
Cable Digital: QAM 256 (Above 30 is good)

Accessing the Service Menu



105-201M

To access the Service Menu.

1) **You must have either Service Remote. p/n 105-201M or p/n MKJ39170828**
2) **Press "In-Start"**
3) **A Password screen appears.**
4) **Enter the Password.**

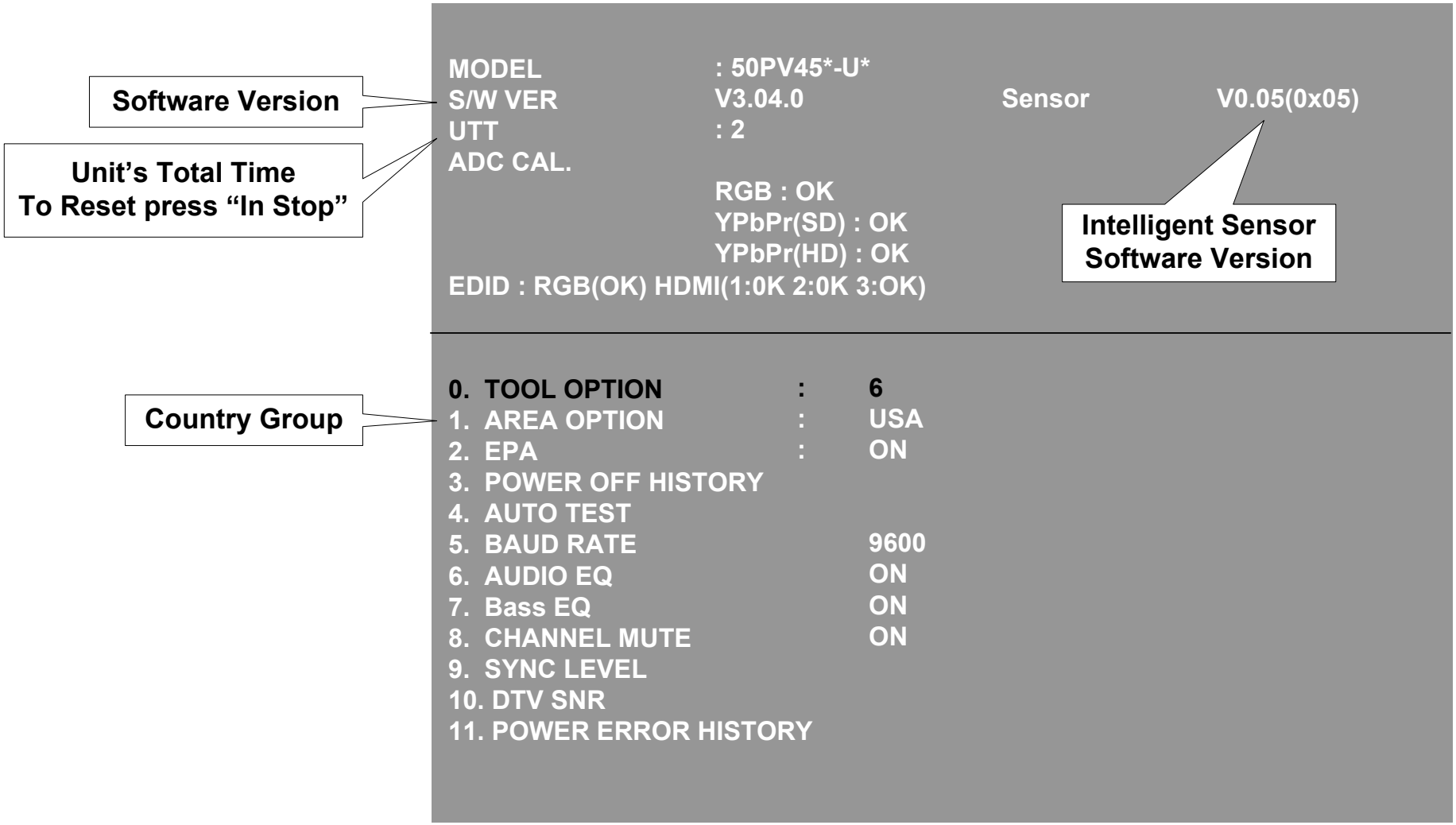
Note: A Password is required to enter the Service Menu. Enter; **0000**

Note: If **0000** does not work use **0413.**

MKJ39170828

50PV450 Service Menu First Page

Bring up the Service Menu using the Service Remote
And pressing “In-Start” enter password 0413.



50PV450 Power Off History

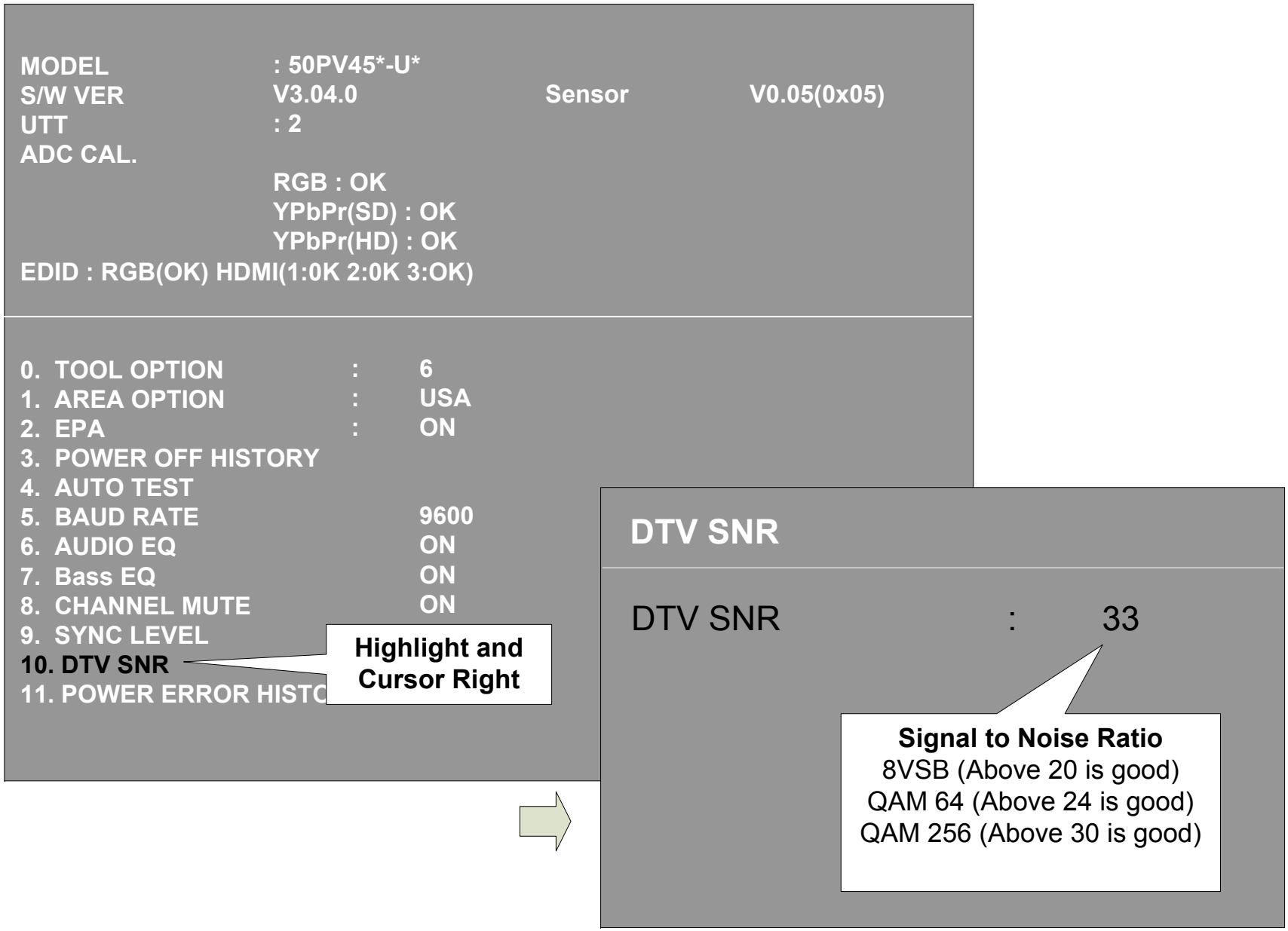
```
MODEL              : 50PV45*-U*
S/W VER            V3.04.0          Sensor     V0.05(0x05)
UTT                : 2
ADC CAL.
                   RGB : OK
                   YPbPr(SD) : OK
                   YPbPr(HD) : OK
EDID : RGB(OK) HDMI(1:0K 2:0K 3:OK)
```

```
0.  TOOL OPTION          :    6
1.  AREA OPTION          :    USA
2.  EPA                  :    ON
3.  POWER OFF HISTORY
4.  AUTO TEST
5.  BAUD RATE                 9600
6.  AUDIO EQ                  ON
7.  Bass EQ                   ON
8.  CHANNEL MUTE              ON
9.  SYNC LEVEL
10. DTV SNR
11. POWER ERROR HISTORY
```

```
POWER OFF HISTORY
LAST HISTORY1      AC DET OFF
LAST HISTORY2      NO SIGNAL OFF
LAST HISTORY3      NO SIGNAL OFF
LAST HISTORY4      ----------
LAST HISTORY5      ----------

RCU OFF            :    0
KEY OFF            :    0
2HOUR OFF          :    0
NO SIGNAL OFF      :    2
AC DEC OFF         :    1
5VMNT OFF          :    0
TVLINK OFF         :    0
CLEAR ALL
```

50PV450 DTV SNR Screen



50PV450 Power Error History

```
MODEL              : 50PV45*-U*
S/W VER            V3.04.0          Sensor     V0.05(0x05)
UTT                : 2
ADC CAL.
                   RGB : OK
                   YPbPr(SD) : OK
                   YPbPr(HD) : OK
EDID : RGB(OK) HDMI(1:0K 2:0K 3:OK)
```

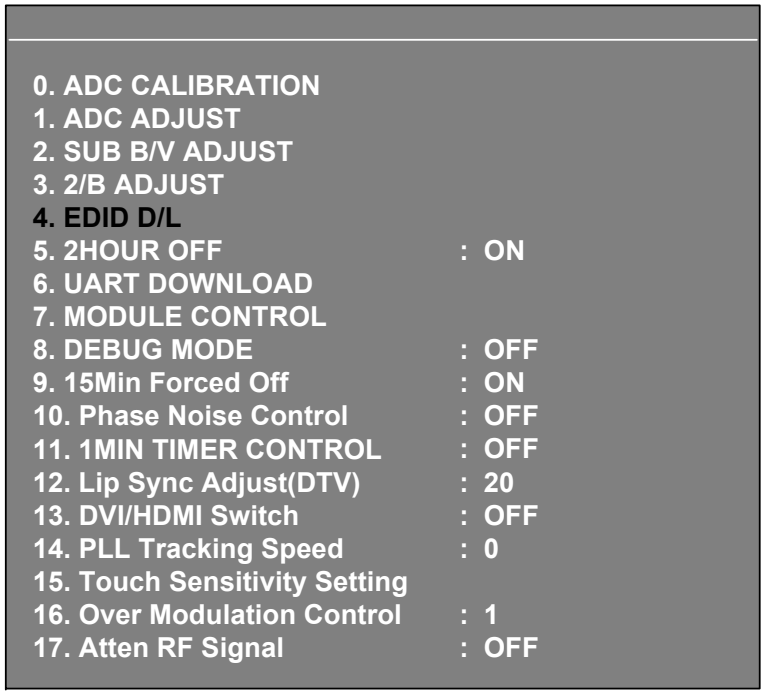
```
0.  TOOL OPTION          :    6
1.  AREA OPTION          :    USA
2.  EPA                  :    ON
3.  POWER OFF HISTORY
4.  AUTO TEST
5.  BAUD RATE                 9600
6.  AUDIO EQ                  ON
7.  Bass EQ                   ON
8.  CHANNEL MUTE              ON
9.  SYNC LEVEL
10. DTV SNR
11. POWER ERROR HISTORY
```

POWER ERROR HISTORY	
LAST HISTORY1	VA UVP
LAST HISTORY2	VS OCP
LAST HISTORY3	----------
PFC_DET Error	0
5V OVP	0
5V UVP	0
17V OVP	0
17V UVP	0
M5V OVP	0
M5V UVP	0
VS OCP	1
VS OVP	0
VS UVP	0
VA OCP	0
VA OVP	0
VA UVP	1
CLEAR ALL	

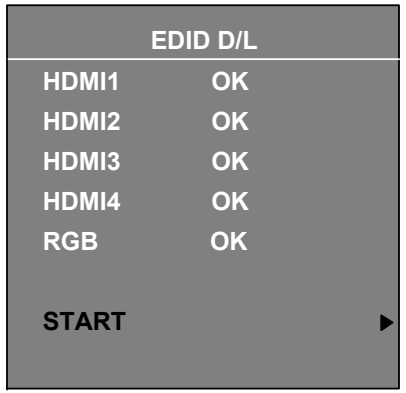
50PV450 Adjust Menu: Downloading EDID Data

1) Press “ADJ” key. Password is required

2) Scroll down and select item 4 EDID D/L



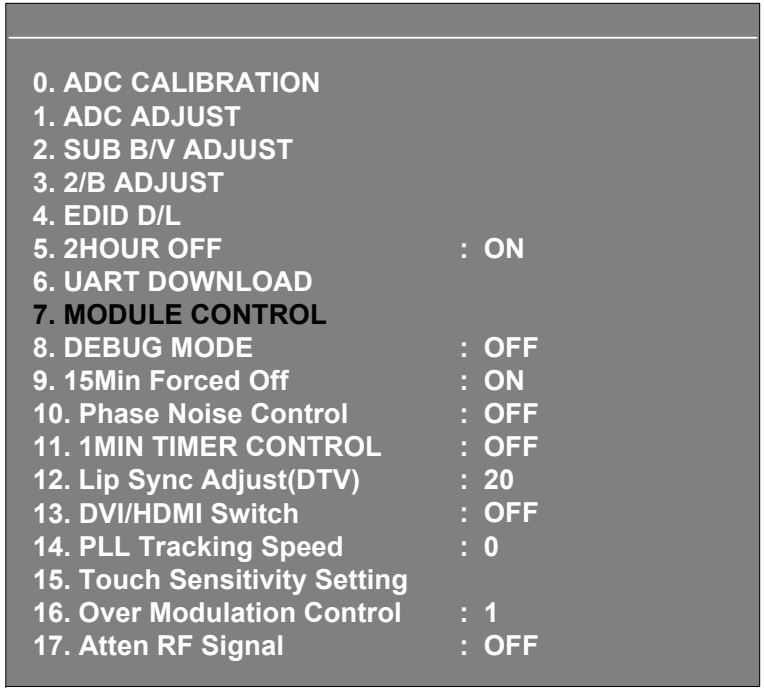
3) In the EDID D/L screen, press the Cursor Right key. EDID data is downloaded.



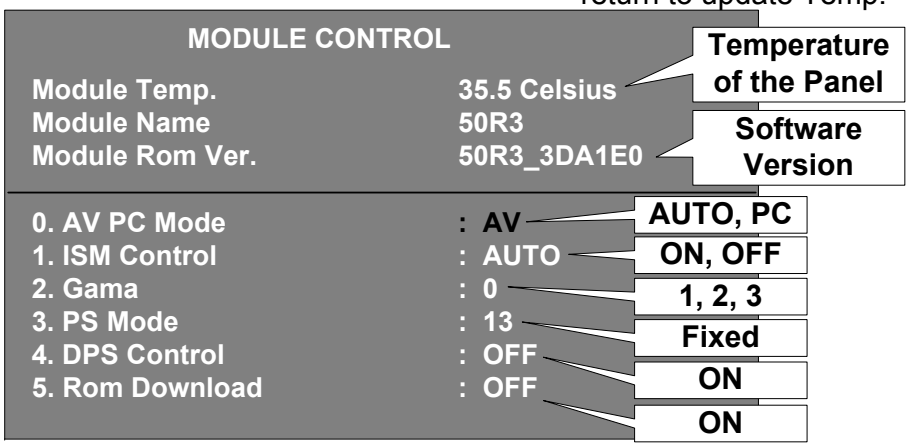
50PV450 Adjust Menu: Module Control Shows Control Board Information

Press the “ADJ” key on the service remote to bring up the Adjust Menu then enter the password.

Item 7 is the Module Control, highlight and cursor right.

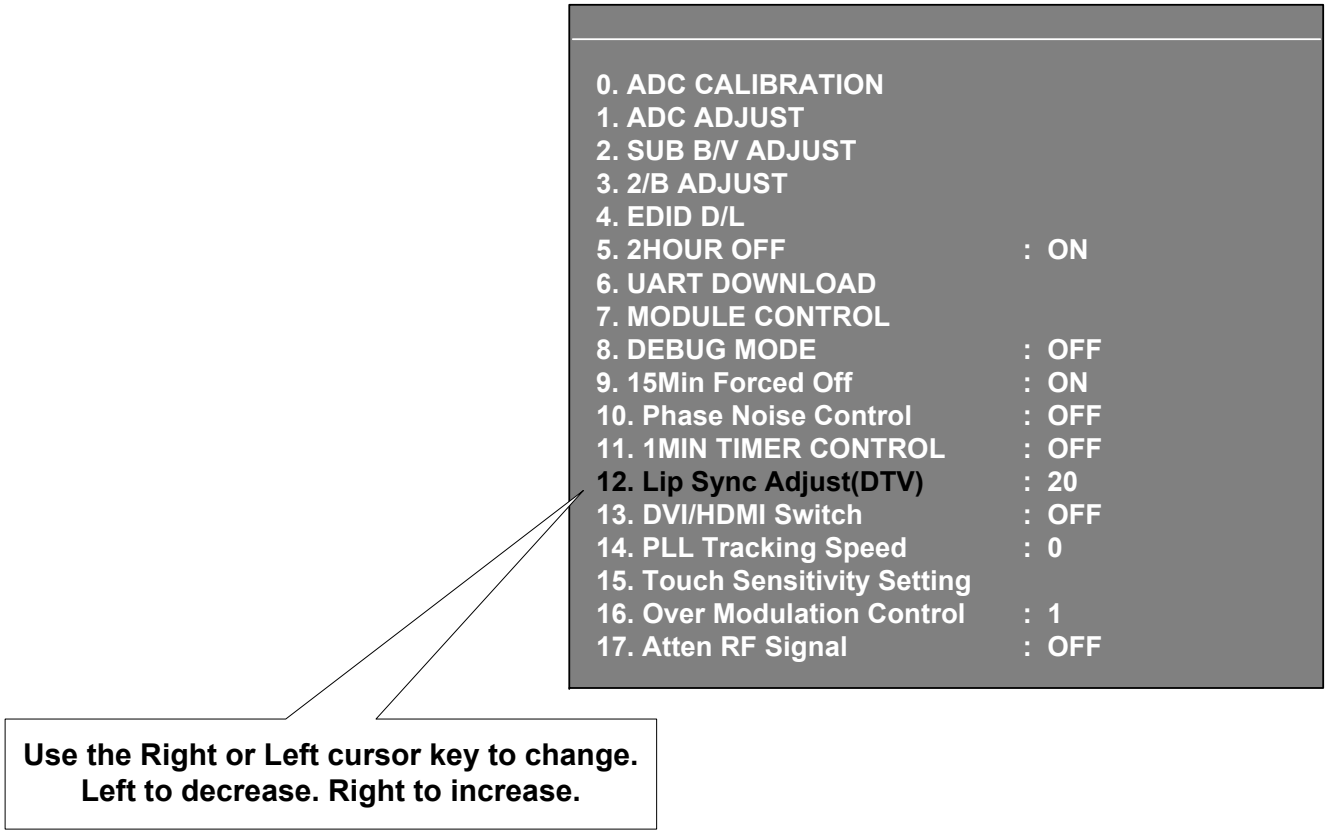


Must leave Adj. Menu and return to update Temp.



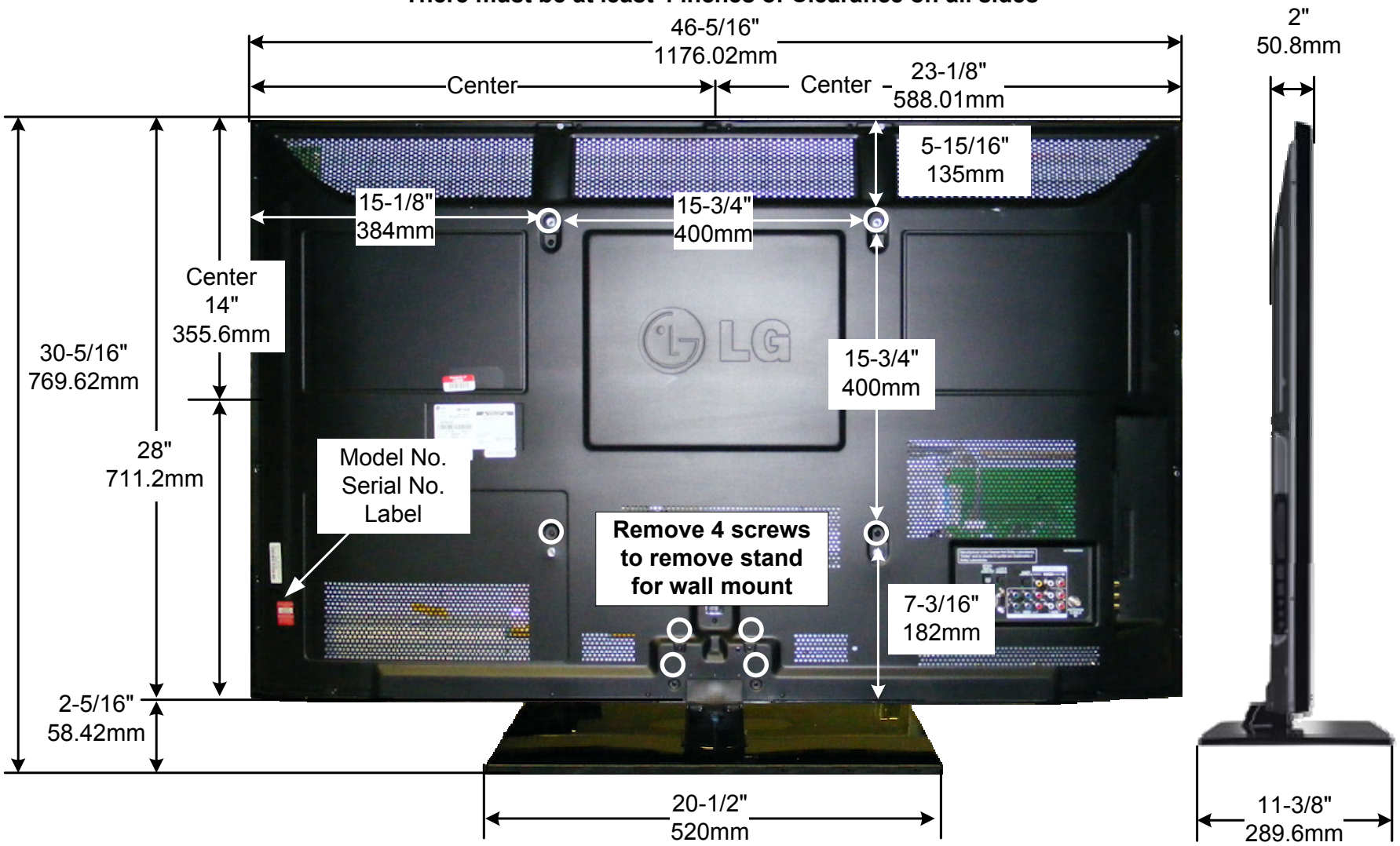
ROM Download when changed to ON blacks out the screen. Press the right cursor key once and 5 seconds later the pix appears.

50PV450 Lip Sync Screens



50PV450 Dimensions

There must be at least 4 inches of Clearance on all sides



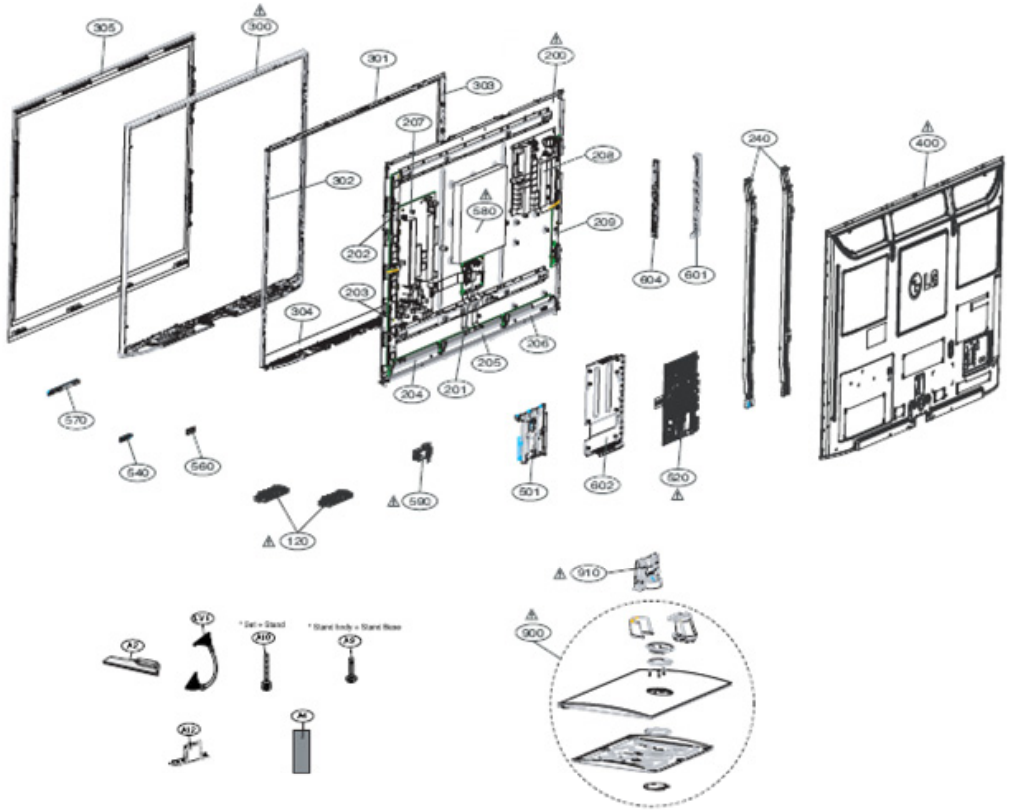
Power Consumption: **Max Watts 270W**
Typical: 145W
<0.2 Watts (Stand-By)

Weight: **65.5 lbs with Stand**
60.4 lbs without Stand

DISASSEMBLY SECTION

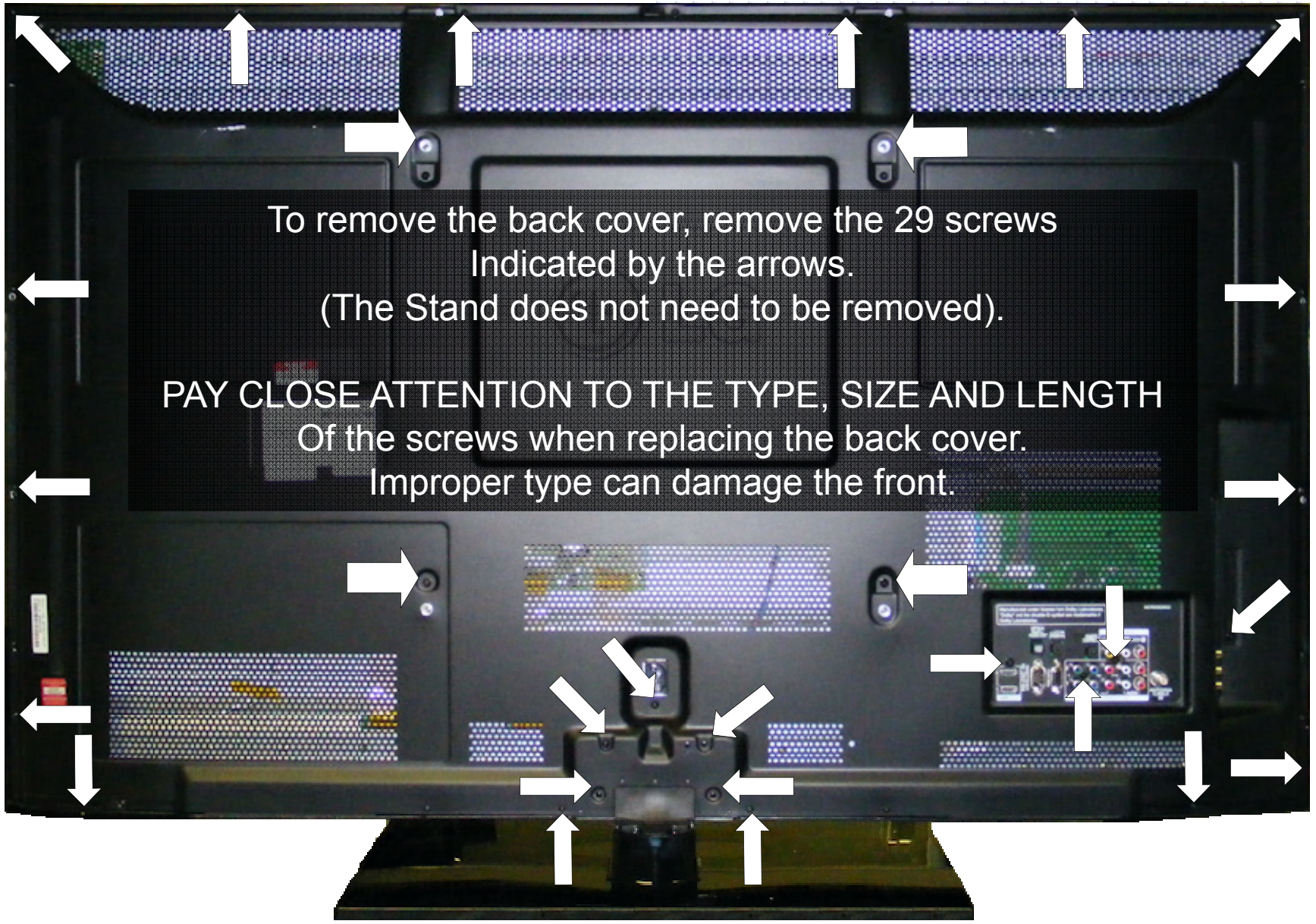
This section of the manual will discuss Disassembly, Layout and Circuit Board Identification of the 50PV450 Advanced Single Scan Plasma Display Panel.

Upon completion of this section the Technician will have a better understanding of the disassembly procedures, the layout of the printed circuit boards and be able to identify each board.



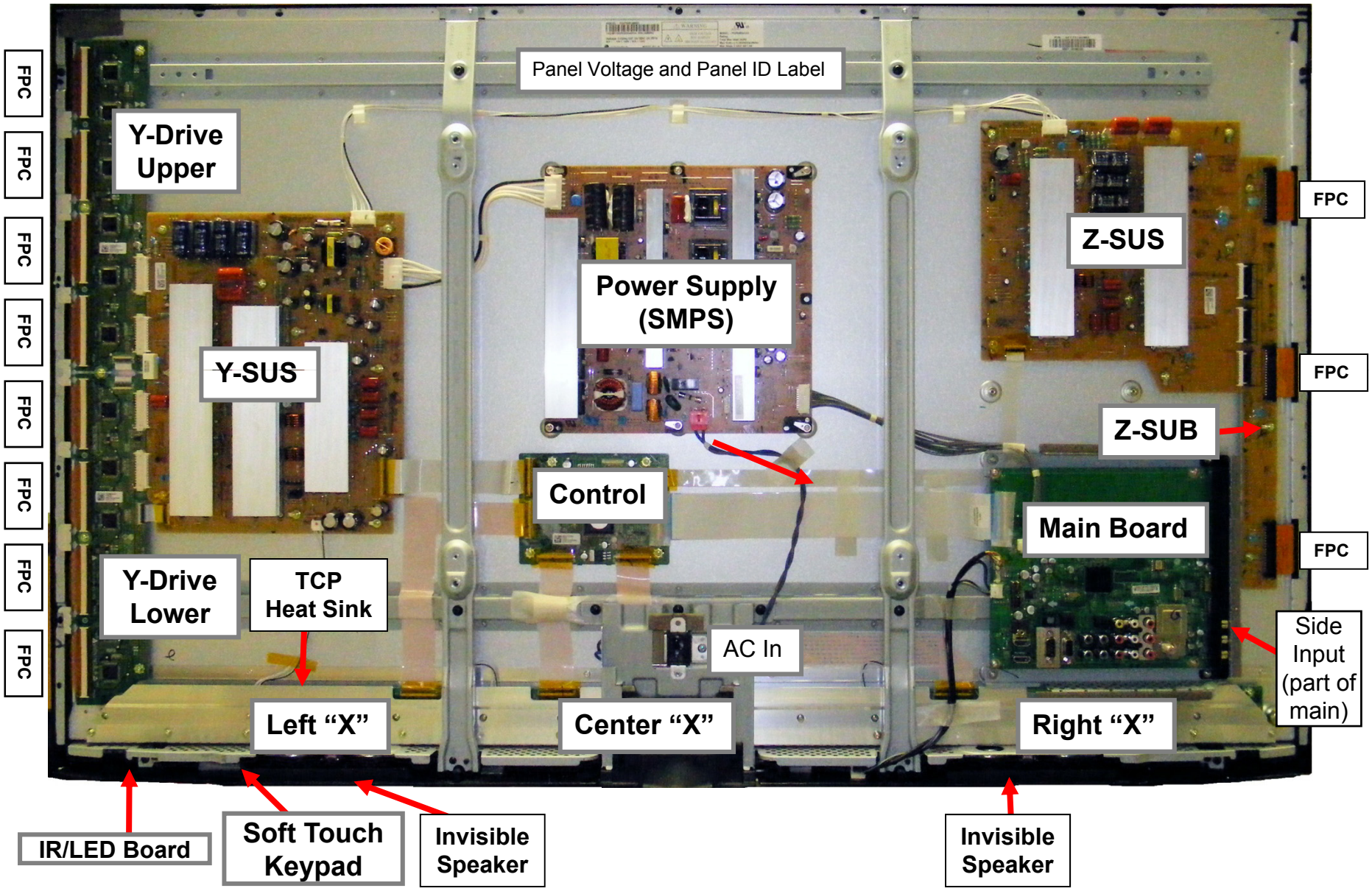
Removing the Back Cover

Caution: Back is metal, it has sharp edges

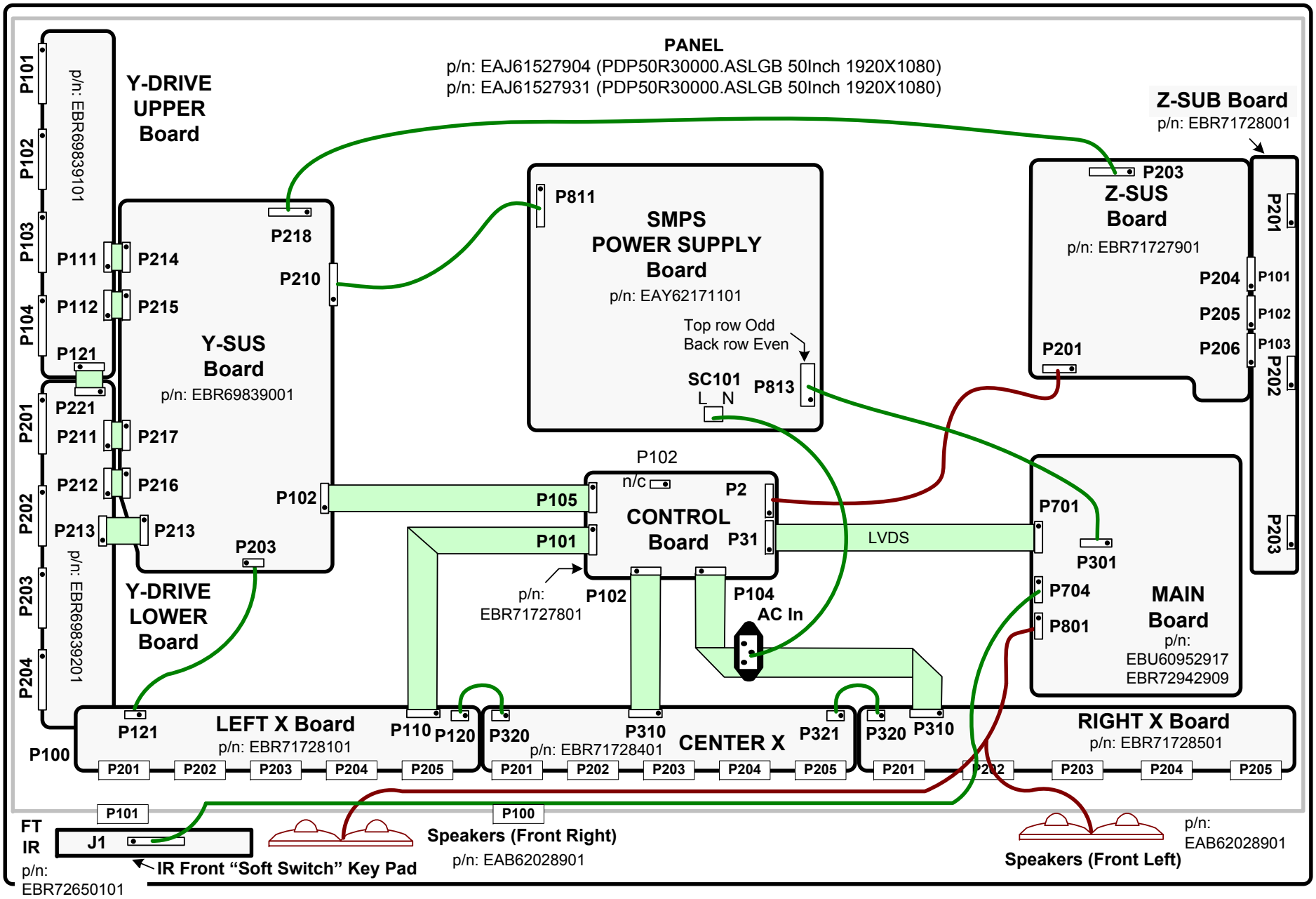


Circuit Board Layout

Identifying the Circuit Boards



50PV450 Connector Identification Diagram



Disassembly Procedure for Circuit Board Removal

Note: Remove AC Power before doing any circuit board removal procedures.

Switch Mode Power Supply Board Removal

Disconnect the following connectors: P811, P813 and SC101.
Remove the 7 screws holding the SMPS in place.
Remove the board.
When replacing, be sure to readjust the Va/Vs voltages in accordance with the Panel Label.
Also, re-confirm VSC, -Vy and Z-Bias as well.

Y-SUS Board Removal

Note: The Y-SUS does not come with the connectors between the Y-SUS and Y-Drive

Disconnect the following connectors: P218, P210 and Ribbon Cables P102 and 213.
Remove the 9 screws holding the Y-SUS in place. ***Do not run the set with P213 or P121/P221 removed.***
Remove the Y-SUS board by lifting up slightly and the carefully unseating connectors P214, P215, P217 and P218 by sliding the Y-SUS to the right while gently prying the connectors apart. When replacing, be sure to readjust the Va/Vs voltages in accordance with the Panel Label. Confirm VSC, -Vy and Z-bias as well.

Y-Drive Boards Removal

Note: The Y-SUS does not come with the connectors between the Y-SUS and Y-Drive

Disconnect the following Flexible Ribbon Connectors P101~P104 and/or P201~P204:
Disconnect the following Connectors P213 and P121/P221 by pressing in on the locking mechanism and lifting upward. ***Do not run the set with these connectors removed.***
Remove the 3 screws holding either of the Y-Drive Boards in place. Lift up slightly, then slide to the left while gently prying the connectors apart. Remove the Y-Drive Board.
Note: Y-SUS, Z-SUS and Y-Drive Boards are mounted on board stand-offs that have a small collar. The board must be lifted slightly to clear these collars. Behind each board are Rubber pieces that act as a cushion. They may make the board stick when removing.

Disassembly Procedure for Circuit Board Removal (Continued)

Z-SUS Board Removal

Disconnect the following connectors: P203 and P201 by lifting up the locking mechanism and unseating.
Remove the 7 screws holding the board in place.
Lift up slightly to clear the screw stand-offs and pull the Z-SUS to the left to unseat P204, P205 and P206 from the Z-SUB board and remove the board.
When replacing, be sure to readjust the Va/Vs voltages in accordance with the Panel Label.
Confirm VS, -Vy and Z-bias as well.

Z-SUB Board Removal

Disconnect the following connectors: P101, P102 and P103 by pulling the locking mechanism to the right and remove the flexible ribbon cables, lifting them up slightly and pulling the FPC out of the connector.
Remove the 3 screws holding the board in place. Lift the board up slightly and slide to the right while unseating P204, P205 and P206. Remove the Z-SUB board.

Main Board Removal

Remove connectors: P701 LVDS (flip the locking tab upward and pulling out the ribbon cable), P301, P704, and P801. Remove the 4 screws holding the Main board in place and Remove the board. Note: After removing the Main board, there is a decorative metal around the bottom left side that must be removed. Release the metal tabs that go through the Main board to remove the piece.

Control Board Removal

Remove the following ribbon cables by flipping the locking tab upward and pulling out the ribbon cables, P31 LVDS, P2, P105, and P101, P102, P104. Remove the 4 screws holding the Control board in place. Lift up and Remove the board. (Note: Chocolate piece behind upper left of board, move to new board).

Front IR / Key Pad / Intelligent Sensor Board

Front IR / Intelligent Sensor and Key Pad Board: (Not Removable) attached to front glass.

X Drive Circuit Board Removal

Remove AC and Lay the Television down carefully on a padded surface.
Make sure to use at least two people for this process so as not to flex the panel glass.
Refer to next 3 pages for disassembly and precautions.

A. Remove the Back Cover.
B. Remove the Stand (4 Stand Screws were removed during back removal).
C. Remove the Stand Metal Support Bracket (5 Screws) 2 Plastic tap thread and 3 Metal thread.
D. Remove the Vertical support Braces.
   Note: There is a Left and a Right brace. (3 Screws per/bracket) 1 Plastic tap thread and 2 Metal thread. (Note: The top screws were removed when the back was taken off).
E. Remove the 13 screws holding the Heat Sink. (Warning: Never run the set with this heat sink removed).
   To remove the heat sink, lift up to release the tacky Chocolate (heat transfer material) and slide the heat sink to the left to clear the connector wires on the right side.
   Note: There may be pieces of conductive tape that may need to be removed.
   Also, note that there are several pieces of Chocolate heat transfer material attached all the way across the underside of the heat sink.

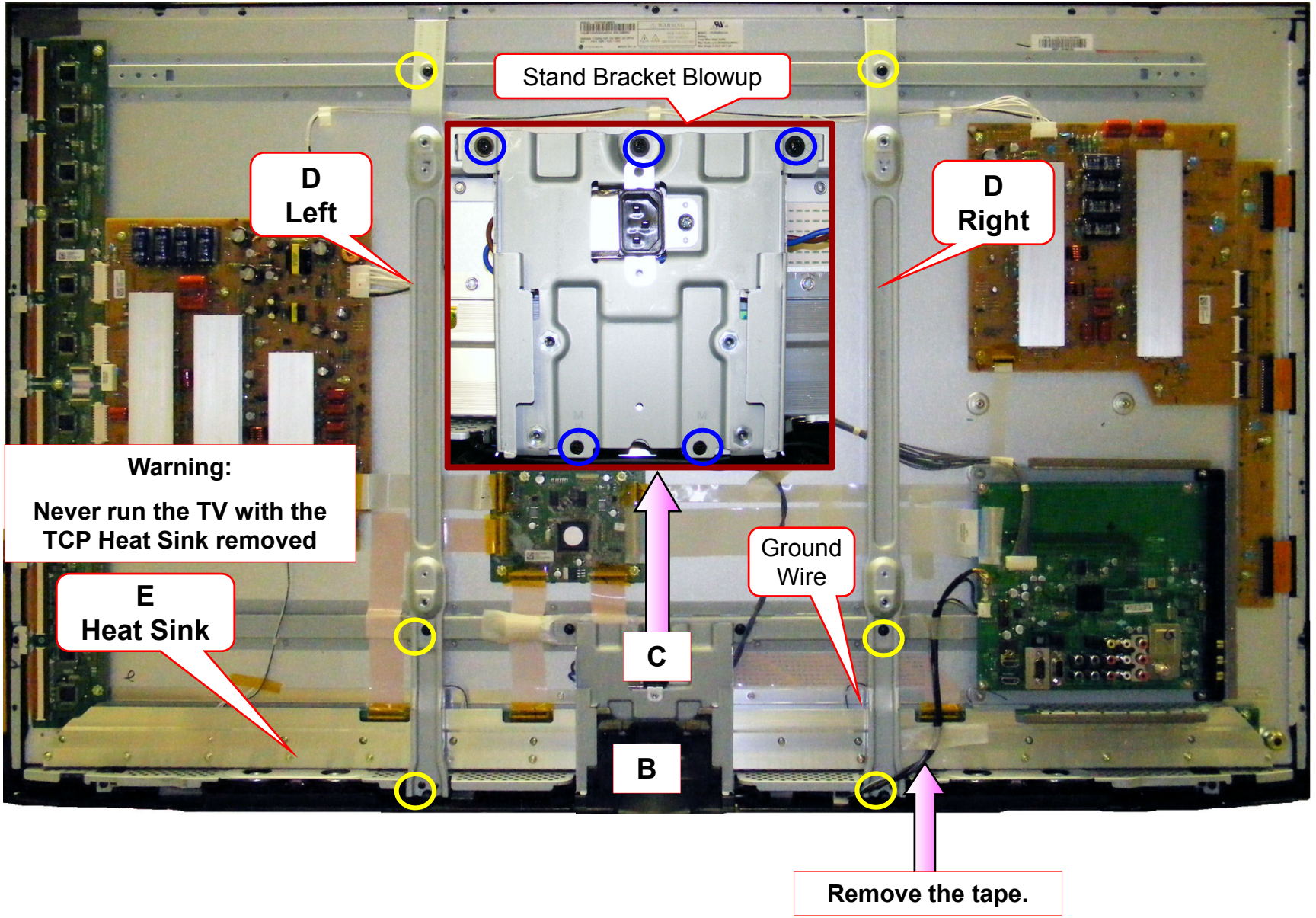
X-DRIVE LEFT, CENTER AND RIGHT REMOVAL:

Disconnect all TCP ribbon cables from the defective X-Drive board and all other Ribbon cables going to the board.

Remove the 5 screws holding the defective X-Drive board in place.

Remove the board. Reassemble in reverse order. Recheck VA / VS / VSC / -VY / Z-Bias.

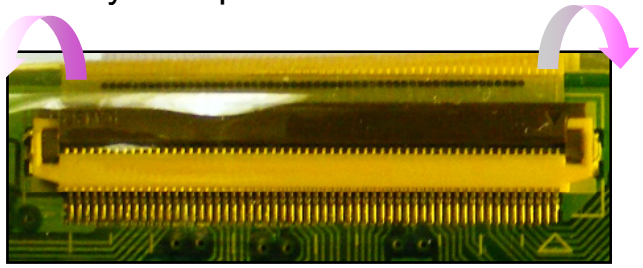
Getting to the X Circuit Boards



Left , Center and Right X Drive Connector Removal

From the Control Board to the X-Boards.
There may be tape on these connectors.

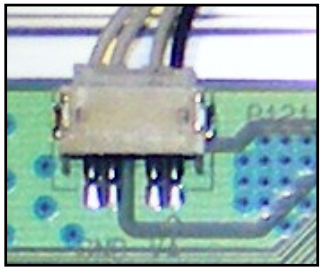
P110
P210
P310
Are all the same



Remove tape (if present) and Gently pry the locking mechanism upward and remove the ribbon cable from the connector.

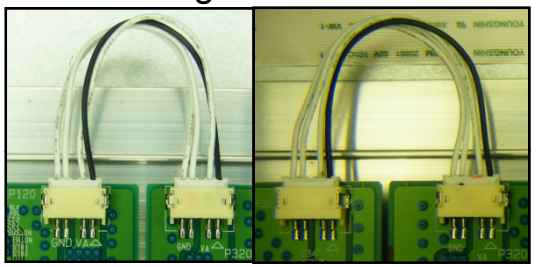
Disconnect connector P121

Va from the Y-SUS to Left X Only



Disconnect Va from Left to Center and Center to Right X Boards

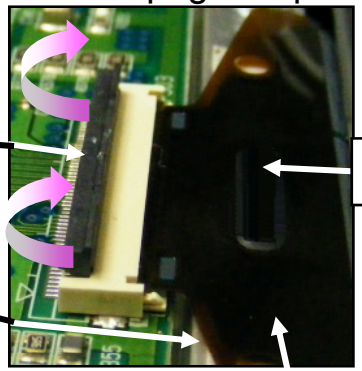
P120 to P220
Left to Center X
P221 to P320
Center to Right X



Removing Connectors to the TCPs.

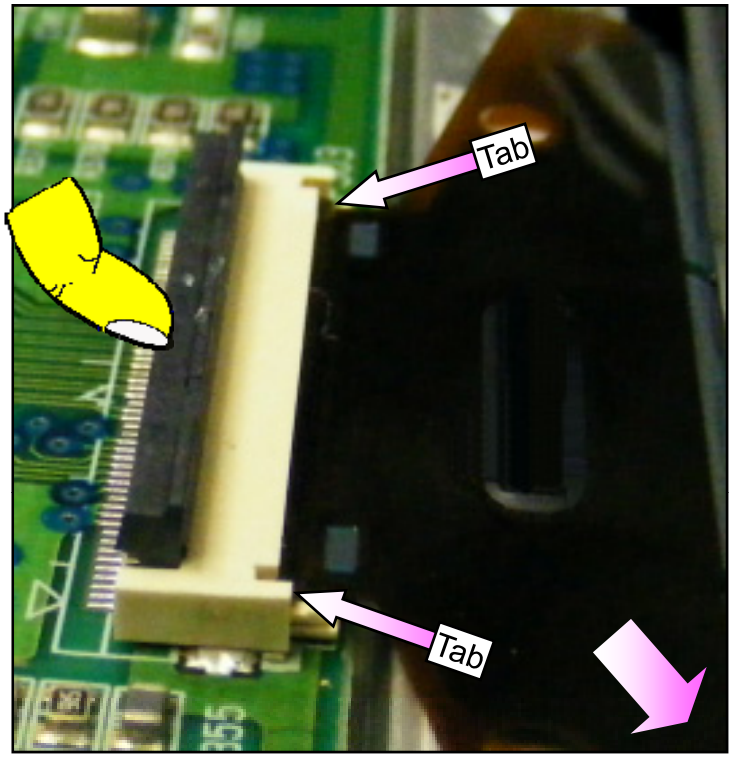
Gently lift the locking mechanism upward on all TCP connectors
Left X: P201~205
Center X: P201~205
Right X: P201~205
And pull the TCP from the connector.

Carefully lift the TCP ribbon up and off.
It may stick, be careful not to crack TCP.
(See next page for precautions)



Flexible ribbon cable connector

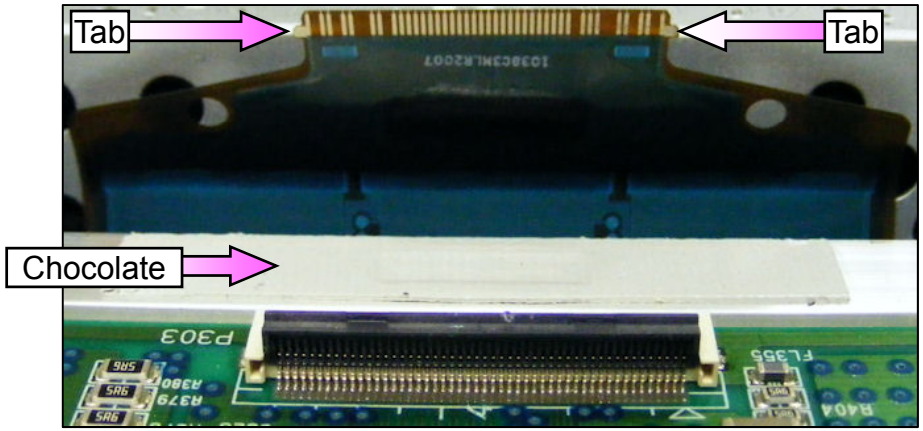
TCP (Tape Carrier Package) Generic Removal Precautions



Lift up the locking mechanism as shown to release the ribbon cable.
(The Lock can be easily damaged, and needs to be handled carefully.)

The TCP Ribbon Cable has two small tabs on each side which help secure it into the connector. They have to be lifted up slightly to pull the Ribbon Cable out.
Note: TCP is usually stuck down to the Chocolate heat transfer material, be Very Careful when lifting up on the TCP ribbon cable.

Separate the TCP Ribbon Cable from the connector as shown.
TCP Film can be easily damaged. Handle with care.



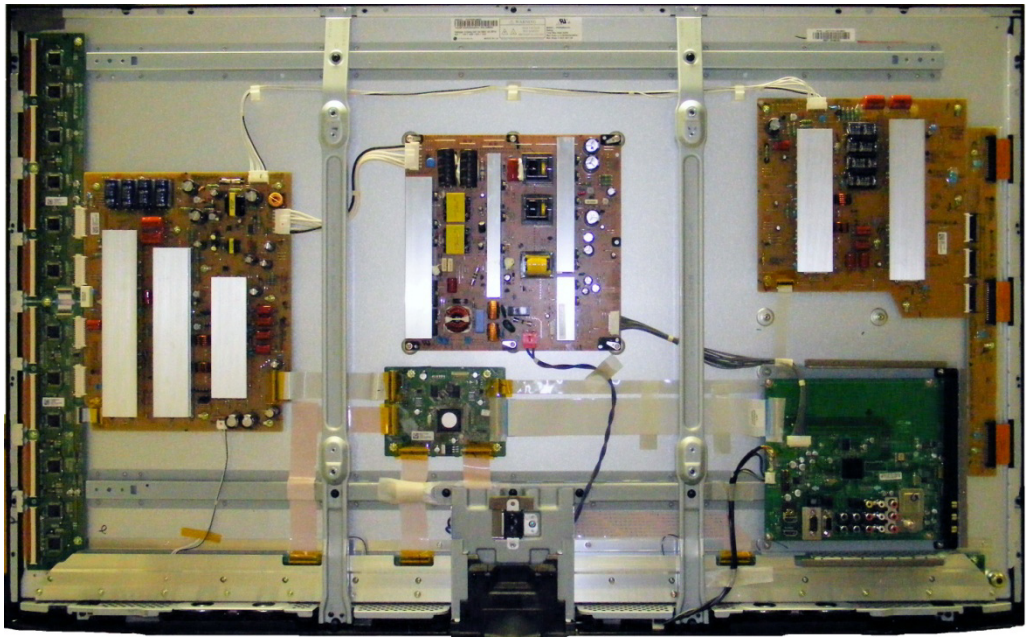
Left, Center and Right X Drive Removal

Remove the screws indicated from the X-Board being removed.

All X-Boards pass R, G, B signals to 5 TCP's across the bottom of the panel.

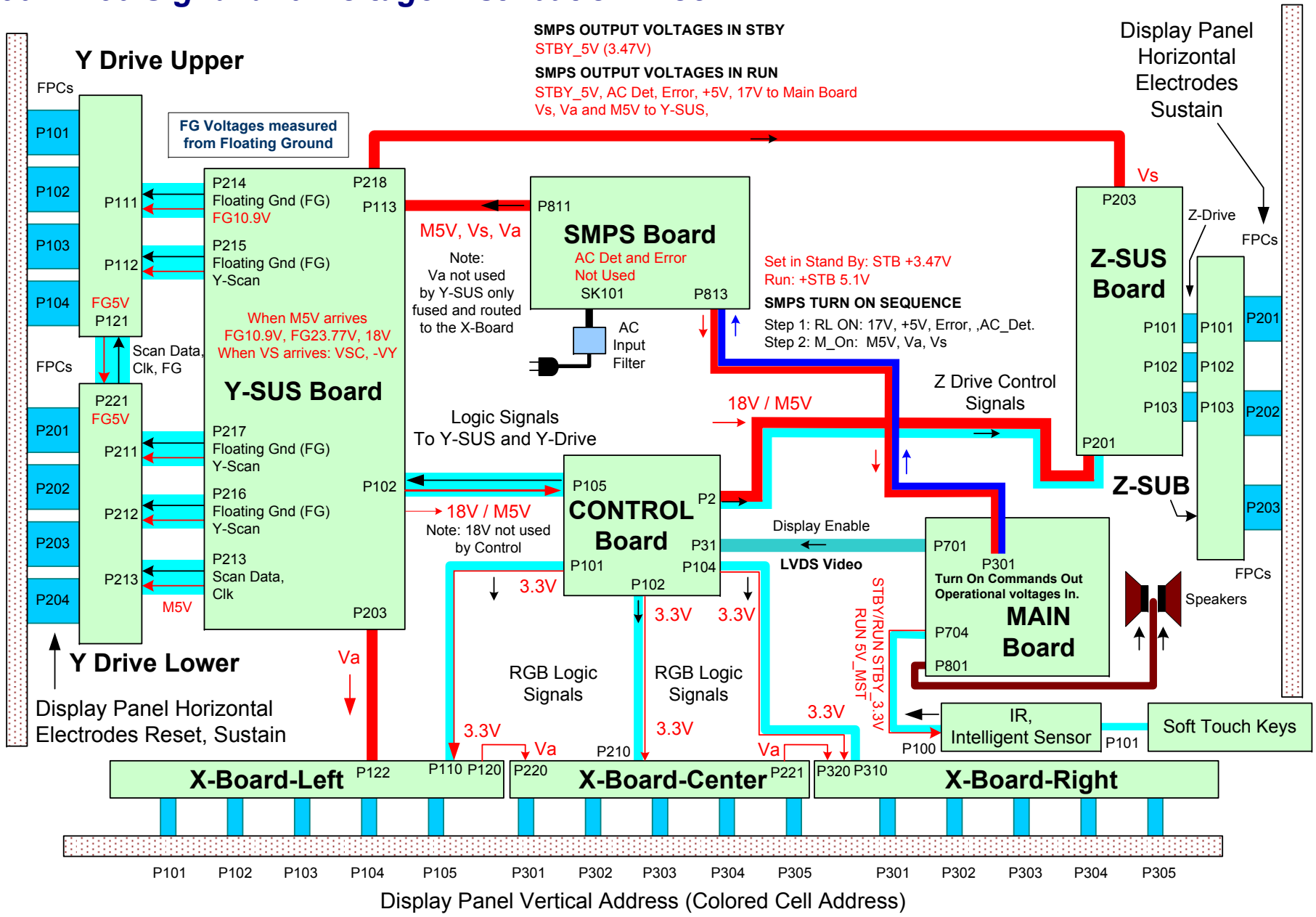
50PV450 Plasma Display

This Section will cover Circuit Operation, Troubleshooting of the Power Supply, Y-SUS Board, Y-Drive Boards, Z-SUS Board, Control Board, Main Board and the X Drive Boards. Alignment of the Power Supply, Y-SUS Board and the Z-SUS Board.

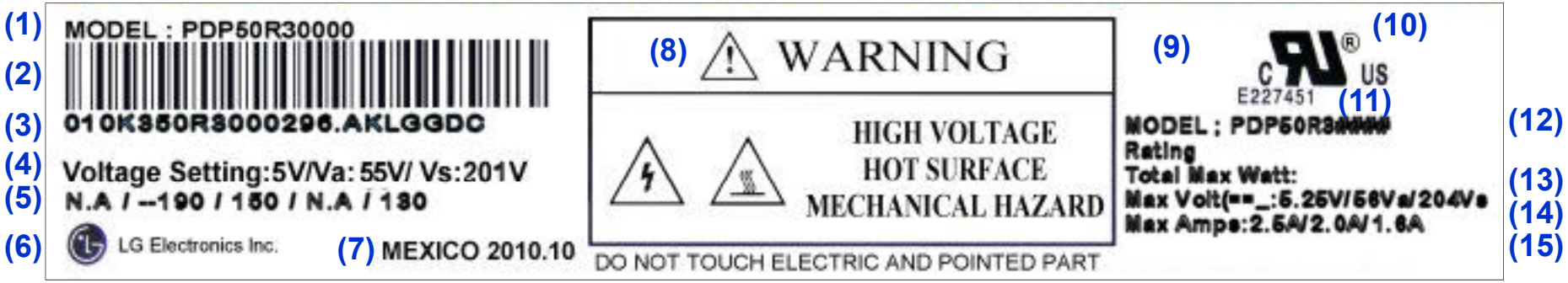


At the end of this Section the technician should understand the operation of each circuit board and how to adjust the controls. The technician should then be able to troubleshoot a circuit board failure, replace the defective circuit and perform all necessary adjustments.

50PV450 Signal and Voltage Distribution Block



Panel Label Explanation



(1) Panel Model Name
(2) Bar Code
(3) Manufacture No.
(4) Adjusting Voltage DC, Va, Vs
(5) Adjusting Voltage (Set Up / -Vy / Vsc / Ve / Vzb)
(6) Trade name of LG Electronics
(7) Manufactured date (Year & Month)
(8) Warning

(9) TUV Approval Mark (Not Used)
(10) UL Approval Mark
(11) UL Approval No.
(12) Panel Model Name
(13) Max. Watt (Full White)
(14) Max. Volts
(15) Max. Amps

Adjustment Notice

All adjustments (DC or Waveform) are adjusted in WHITE WASH.
Customer's Menu, Select "Options", select "ISM" select "WHITE WASH".

It is critical that the DC Voltage adjustments be checked when;

1) **SMPS, Y-SUS or Z-SUS board is replaced.**
2) **Panel is replaced, Check Va/Vs since the SMPS does not come with new panel**
3) **A Picture issue is encountered**
4) **As a general rule of thumb when ever the back is removed**

ADJUSTMENT ORDER "IMPORTANT"

DC VOLTAGE ADJUSTMENTS

1) **POWER SUPPLY: VS, VA** (Always do first)
2) **Y-SUS: Adjust –Vy, VSC**
3) **Z-SUS: Adjust Z-Bias (VZB)**

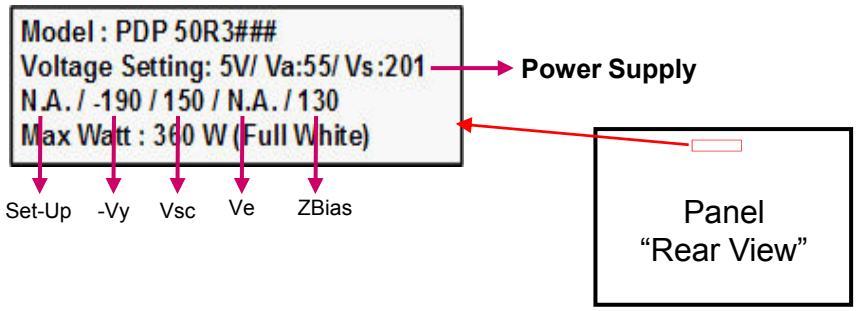
WAVEFORM ADJUSTMENTS

1) **Y-SUS: Set-Up, Set-Down**

The Waveform adjustment is only necessary

1) When the Y-SUS board is replaced
2) When a "Mal-Discharge" problem is encountered
3) When any abnormal picture issue is encountered

Remember, the Voltage Label MUST be followed, it is specific to the panel's needs.



All label references are from a specific panel. They are not the same for every panel encountered.

SWITCH MODE POWER SUPPLY SECTION

This Section of the Presentation covers troubleshooting the Switch Mode Power Supply. Upon completion of the section the technician will have a better understanding of the operation of the Power Supply Circuit and will be able to locate test points needed for troubleshooting and alignments.

- DC Voltages developed on the SMPS
- Adjustments VA and VS.

Always refer to the Voltage Sticker on the back of the panel, located at the upper Center, for the correct voltage levels for the VA and VS supplies as these voltages will vary from Panel to Panel even on the same Model.

SMPS P/N EAY62171101
Check the silk screen label on the top center of the Power Supply board to identify the correct part number. (It may vary in your specific model number).

On the following pages, we will examine the Operation of this Power Supply.

Switch Mode Power Supply Overview

SMPS p/n: EAY62171101

The Switch Mode Power Supply Board Outputs to the :

Y-SUS Board	**VS**	**Drives the Display Panel's Horizontal Electrodes.**
	VA	**To Y-SUS, fused then to the X-Boards. (Not used by Y-SUS). Primarily responsible for Display Panel Vertical Electrodes.**
	M5V	**Used to develop Bias Voltages on the Y-SUS, Z-SUS Boards.**

Y-SUS Delivers VS to Z-SUS Board

	VS	**Drives the Display Panel's Horizontal Electrodes.**

Main Board	**STBY 5V**	**Microprocessor Circuits**
	17V	**Audio B+ Supply, Tuner B+ Circuits**
	5V	**Signal Processing Circuits**
		AC_Det and Error_Det.

Adjustments

There are 2 adjustments located on the Power Supply Board VA and VS. The M5V is pre-adjusted and fixed. All adjustments are made referenced to Chassis Ground. Use "Full White Raster" 100 IRE

VS	**VR901**
VA	**VR501**

50PV450 SMPS Layout Drawing

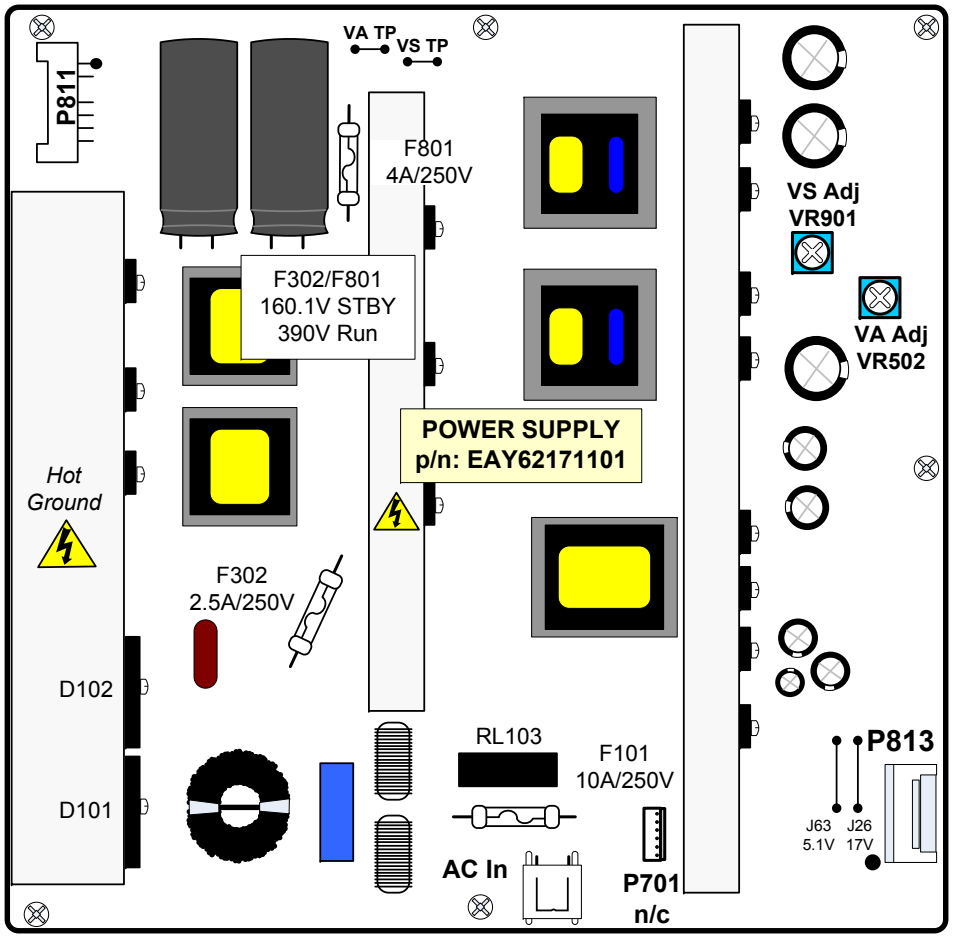
P811
1) VS
2) VS
3) n/c
4) Gnd
5) Gnd
6) VA
7) M5V

VS or VA Diode Check
Open with Board Disconnected or
Open with Board Connected

M5V Diode Check
0.73V Board Connected or
0.72V Disconnected

CURRENT LABEL

Input: 100~240V 50/60Hz 4.8A
17V= 1A
5.1V = 3.0A
STBY5V (5V) = 1A
VS 201~207V = 1.6A
VA 55V = 2.0A
M5V (5.1V) = 2.5A
PDP Module MAX 360W



Example Panel Label:

Model : PDP 50R3###
Voltage Setting: 5V/ Va:55/ Vs:201
N.A. / -190 / 150 / N.A. / 130
Max Watt : 360 W (Full White)

VA **VS**

P813 "SMPS" to P301 "Main"

Pin	Label	Stby	Run	Diode
18	[e]Auto_Gnd	Gnd	Gnd	Gnd
17	[b]M_On	0V	3.28V	Open
16	[a d]AC_Det	0V	4.06V	3.1V
15	[a]RL_ON	0V	3.28V	Open
13-14	Stby_5V	3.47V	5.14V	2.53V
9-12	Gnd	Gnd	Gnd	Gnd
8	[a c]Error_Det	3.44V	4.02V	2.84V
5-7	[a]5.1V	0.46V	5.17V	2.13V
3-4	Gnd	Gnd	Gnd	Gnd
1-2	[a]17V	0V	17V	3.06V

Note a:
The RL_On command turns on the 17V, +5V, Error_Det and AC_DET.

Note b:
The M-On command turns on M5V, Va and Vs.

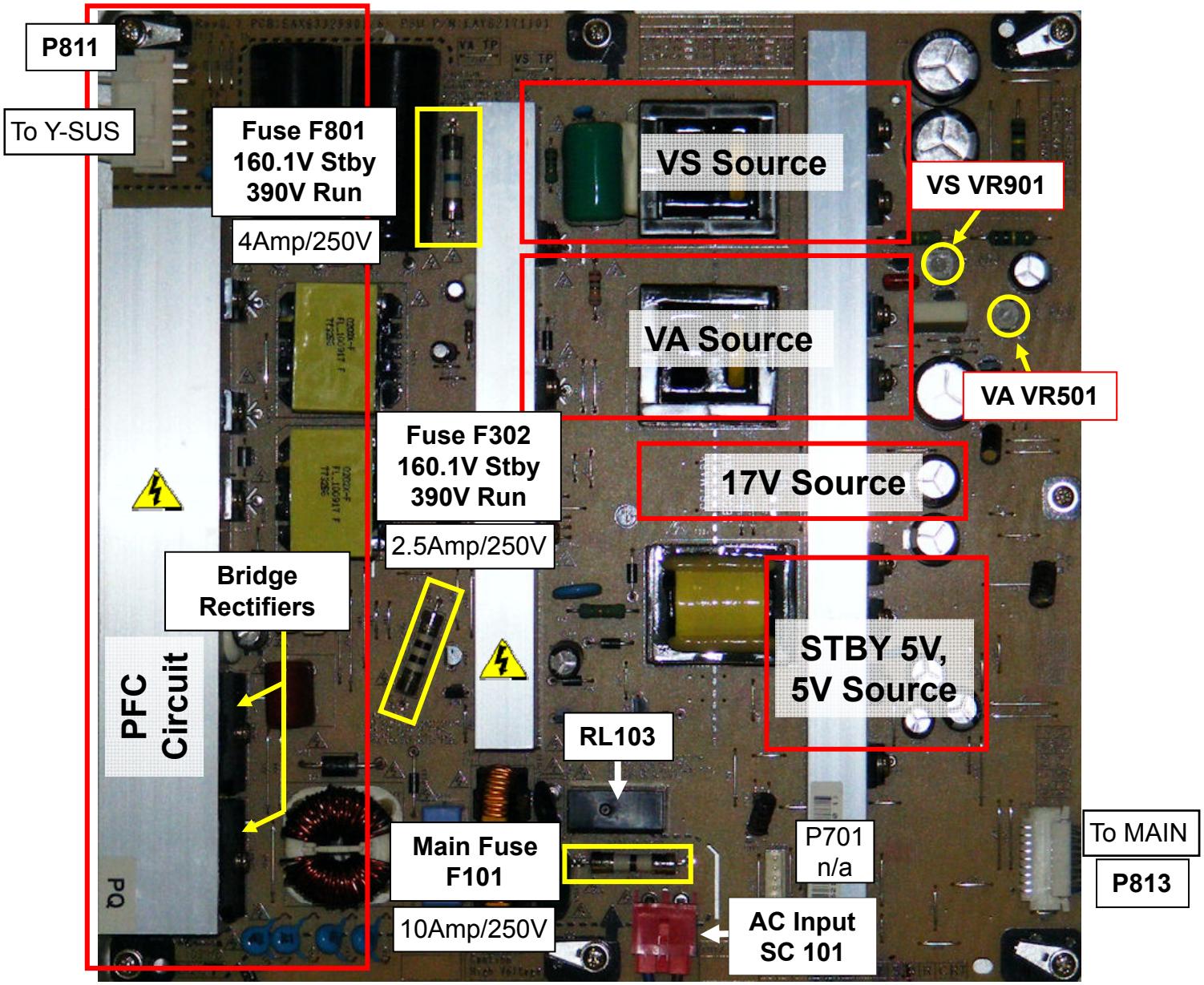
Note c:
The Error Det line is not used in this model.

Note d:
AC Det line is not used.

Note e:
Pin 18 is grounded on the Main. If opened, the power supply turn on automatically.

Power Supply Circuit Layout

SMPS p/n: EAY62171101



Power Supply Basic Operation

AC Voltage is supplied to the SMPS Board at Connector SC101 from the AC Input assembly, routed to the two Bridge Rectifiers D101 and D102 which then route the primary voltage to the PFC circuit (Power Factor Controller). Standby 5V is developed from 160.1V source supply (which during run measures 390V measured from the primary fuses F801 and F302). This supply is also used to generate all other voltages on the SMPS.
The STBY5V (standby) is B+ for the Controller chip on the back of the SMPS board (IC701) and output at P813 pins 13 and 14 then sent to the Main board for Microprocessor (IC600) operation (STBY 3.47V RUN 5.14V).

When the Microprocessor (IC1 on the Main Board) receives a “POWER ON“ Command from either the Power button or the Remote IR Signal, it outputs a high (2.4V) called **RL_ON** at Pin 15 of P301 to P813 on the SMPS. This command causes the Relay Circuit to close Relay RL103 bringing the PFC circuit up to full power by increasing the 160V standby to 390V run which can be read measuring voltage at Fuse F302 and F801 (390V) from “Hot” Ground. AC Detection (AC Det) is generated on the SMPS, by rectifying a small sample of the A/C Line and routed to the Controller (IC701) where it outputs at P813 pin 16 (4.4V) called AC_DET. and sent to P301 to the Main Board. If missing, the TV will attempt to turn on, but will shut right back off.

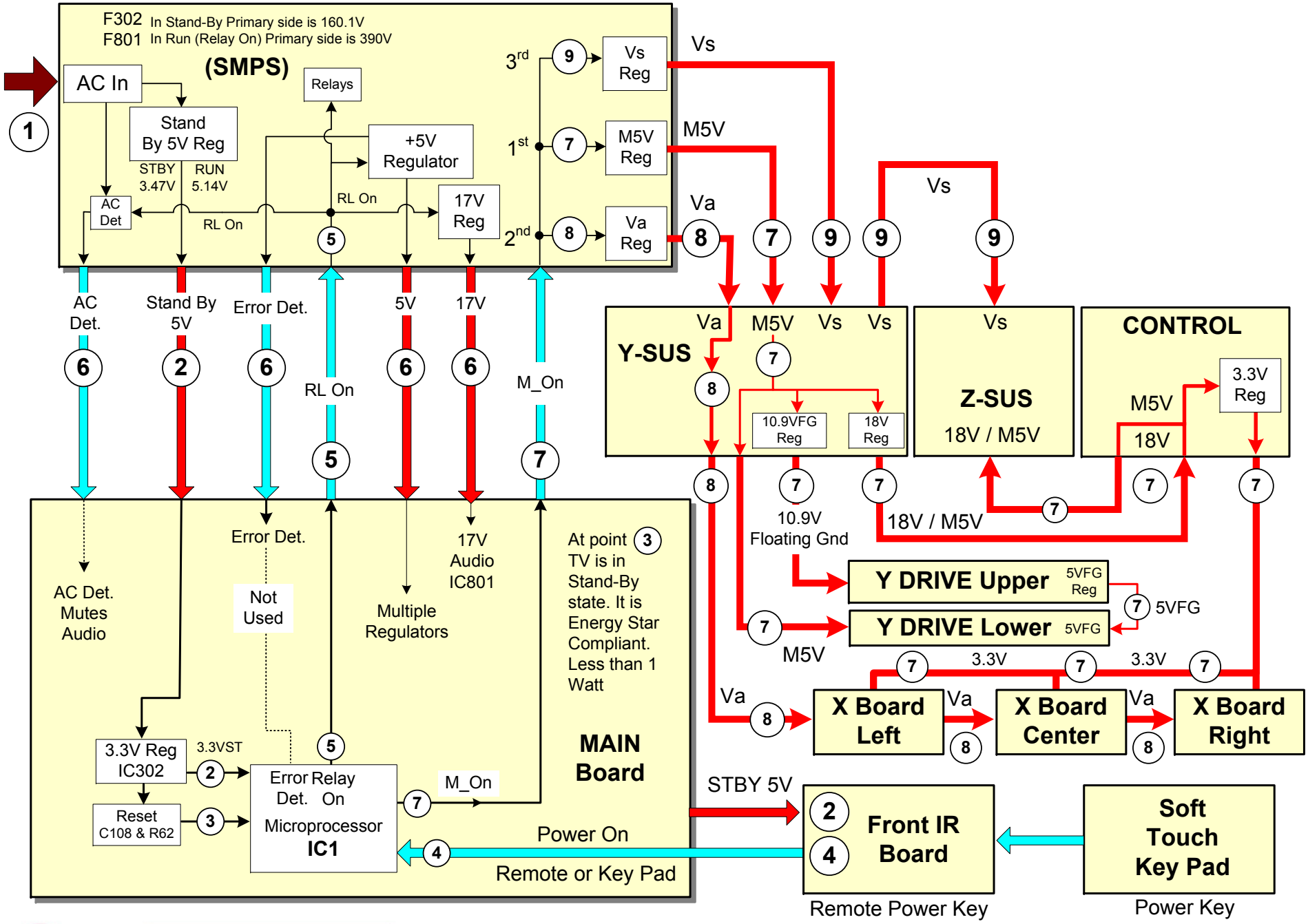
When **RL_ON** arrives, the run voltage +5V source becomes active and is sent to the Main Board via P813 (+5.1V at pin 5, 6 and 7). The (Error Det) from the SMPS Board to the Main Board can be measured at pin 8 of P813 (2.87V STBY and 4.9V RUN), but it is not used. The **RL-ON** command also turns on the 17V (Audio B+) which is also sent to the Main Board. The 17V (17V) Audio supply outputs to the Main board at P813 pins 1 and 2 and used for Audio processing.

The next step is for the Microprocessor on the Main Board to output a high (3.2V) on **M_ON** Line to the SMPS at P813 Pin 17 which is sensed by the Controller IC701, turning on the M5V line and outputs at P811 pin 7 to the Y-SUS board.

The Controller (IC701) also uses the **M_ON** line to turn on the VA and the VS supplies. (Note there is no VS On Command in this set). VS is output at P811 to the Y-SUS board P210.
(VA pins 6 and VS pins 1 and 2). Note: The Va is fused (FS203) on the Y-SUS then routed out P203 pins 4-5 to the X-Board Left. Vs is routed out of the Y-SUS P218 pins 4-5 to P203 on the Z-SUS where it is fused by FS201.

AUTO GND Pin 18 of P813: This pin is grounded on the Main board. When it is grounded, the Controller (IC701) works in the normal mode, meaning it turns on the power supply via commands sent from the Main board. When **AUTO GND** is floated (opened), it pulls up and places the Controller (IC701) into the Auto mode. In this state, the Controller turns on the power supply in stages automatically. A load is necessary to perform a good test of the SMPS if the Main board is suspect.

50PV450 Television Turn On Sequence



Turn On Sequence Text

The text below is related to the previous page.

STBY 5V (Stepped down to 3.3V_ST by IC302) powers on the Microprocessor IC1 on the Main board. This also starts the 12Mhz Oscillator (X1) however, the Microprocessor is not functional until after it is Reset. The Reset circuit (C108 and R62) is energized when 3.3V_ST arrives.

AC Det is 0V when the set is in Stand-By, but rises to 4.4V when the set turns on by the Relay-On Command. AC Det is not used in this set, however if missing it will Mute the Audio.

At power on the 1st output from the Microprocessor (IC1) is the Relay On command called (RL-ON) which turns on the following SMPS supplies: +5V for Video Processing 17V for Audio Amplification.
On the Main board the 17V is sent to the Audio Amp (IC801).
The SMPS (+5V) creates a signal called (ERROR DET) and is sent to the Main Board but it is not used by the Main board.

The 2nd output from the Microprocessor is the (M_ON) command which turns on (3) supplies:

(1) M5V (Monitor 5V): For the Control Board, Y-SUS Board, Lower Y-Drive and Z-SUS Board. (The M5V is routed through the Y-SUS to the Control Board then to the Z-SUS and through the Y-SUS to the Lower Y-Drive).

(2) Va: (Voltage for Address) For amplification voltage for the TCPs driving the vertical electrodes. (Voltage routed through the Y-SUS then to the X-Drive boards.

(3) Vs: Voltage for Sustain sent to the Y-SUS and then to the Z-SUS) used for amplification voltage driving the horizontal electrodes.

On the Y-SUS, when M5V arrives, it develops 3 voltages: FG23V, FG10.9V (FG=Floating Ground) and 18V.
The 18V is routed through the Control board to the Z-SUS. The FG10.9V is routed to the upper Y-Drive board and regulated down to FG5V and used by both the upper and lower Y-Drive boards for the low voltage processing voltage.
When Vs arrives on the Y-SUS, it develops 2 additional voltages; -Vy and VSC which are adjustable.

When the M5V from the SMPS through the Y-SUS arrives on the Control board, the control develops 3.3V and 1.8V for internal use and 3.3V which is routed down to the each X-Board for each TCP's low voltage processing voltage.

Power Supply Va and Vs Adjustments

Important: Use the Panel Label
Not this book for all voltage adjustments.

Use Full White Raster "White Wash"

Example Voltage Label

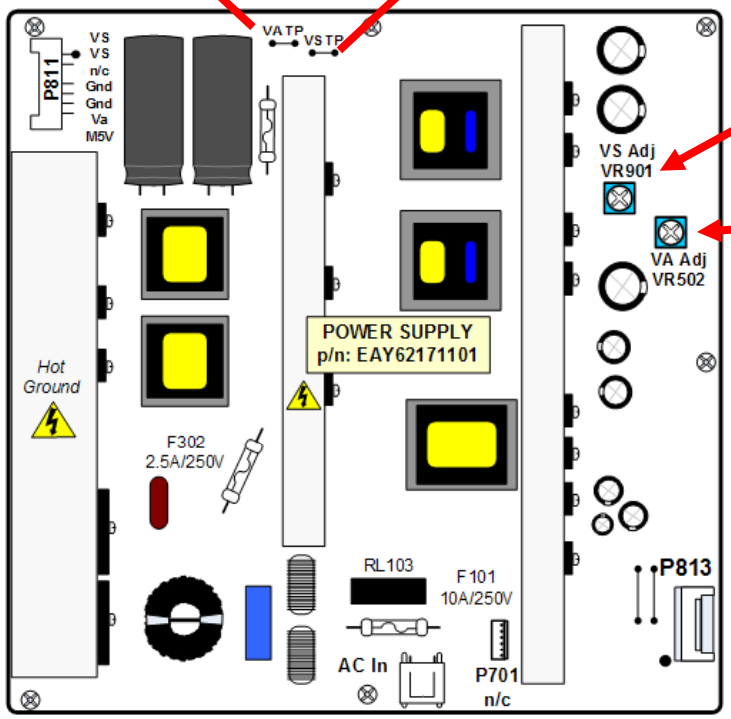
Model : PDP 50R3###
Voltage Setting: 5V/ Va:55/ Vs:201
N.A. / -190 / 150 / N.A. / 130
Max Watt : 360 W (Full White)

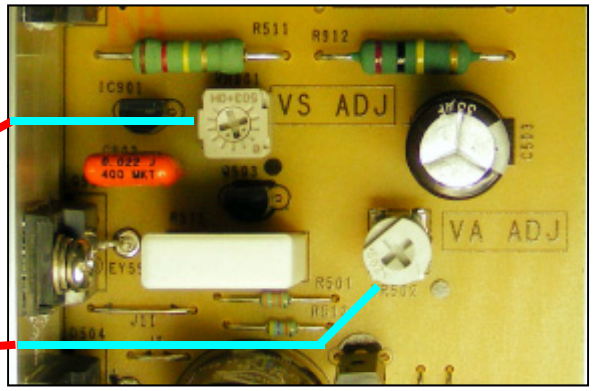
VA Voltage

VS Voltage

Va TP or P811 Pin 5

Vs TP or P811 Pin 1 or 2



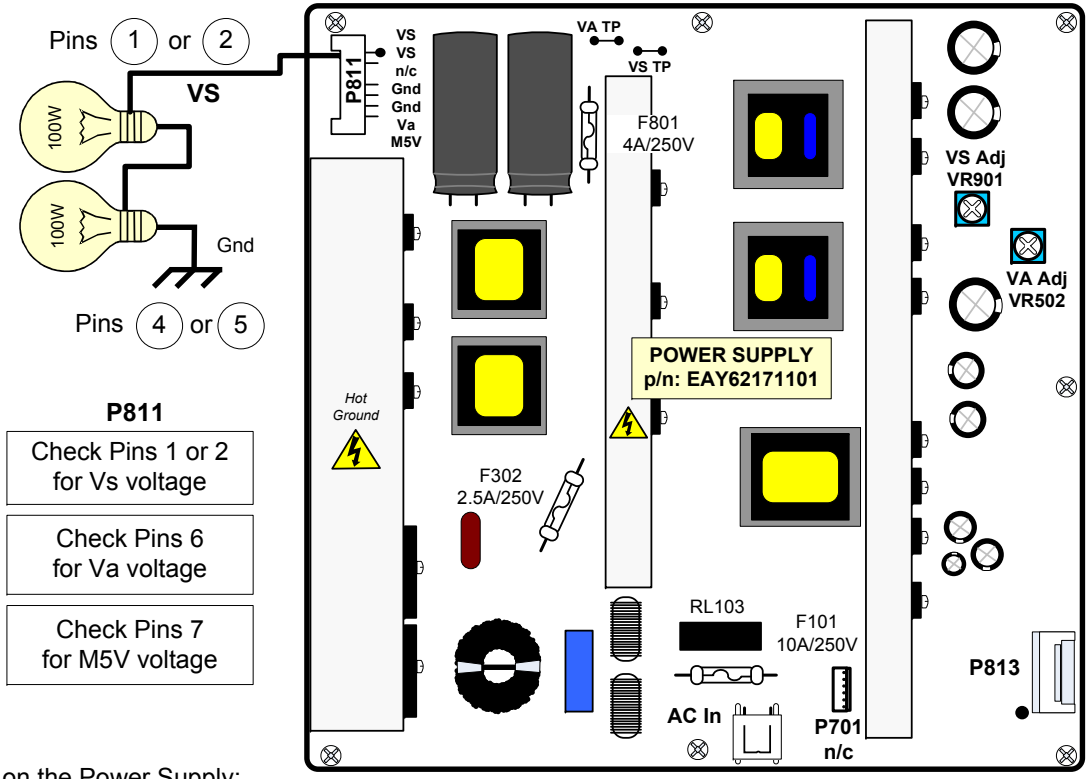


Vs Adjust:
Place voltmeter on VS TP.
Adjust VR901 until the reading matches your Panel's label.

Va Adjust:
Place voltmeter on VA TP.
Adjust VR502 until the reading matches your Panel's label.

Power Supply Static Test with Light Bulb Load

Using two 100 Watt light bulbs, attach one end to Vs and the other end to ground. Apply AC to SC101. If the light bulbs turn on and VS is the correct voltage, allow the SMPS to run for several minutes to be sure it will operate under load.
If this test is successful and all other voltages are generated, you can be fairly assured the power supply is OK.
Note: To be 100% sure, you would need to read the current handling capabilities of each power supply listed on the silk screen on the SMPS and place each supply voltage under the appropriate load.



P811

Check Pins 1 or 2 for Vs voltage
Check Pins 6 for Va voltage
Check Pins 7 for M5V voltage

P813

Check Pins 1 or 2 For 17V (17V)
Check Pin 5,6 and 7 for (+5.22V)
Check Pin 8 for Error Det (4.94V)
Check Pins 13 or 14 for 5V SBY (4.94V)
Check Pin 16 for AC Det (4.94V)

Note:
Always test the SMPS under a load using the 2 light bulbs.
Abnormal operational conditions may result if not loaded.

CURRENT LABEL

Input: 100~240V 50/60Hz 4.8A
17V= 1A
5.1V = 3.0A
STBY5V (5V) = 1A
VS 201~207V = 1.6A
VA 55V = 2.0A
M5V (5.1V) = 2.5A
PDP Module MAX 360W

Note:
To turn on the Power Supply;
1) With Main Board connected, press power.
2) Without Main Board connected SMPS will turn on automatically.

Any time AC is applied to the SMPS,
STBY 5V will be 3.47V and will be 5.14V when the set turns on.
AC_DET WILL NOT be present until set comes on, but it's not used. If AC_DET is missing to the Main board, it will Mute the Audio.
Error line WILL NOT be present until set comes on, but it's not used.

Power Supply Static Test (Forcing on the SMPS in stages)

WARNING: Remove AC when adding or removing any jumper, plug or resistor.

TEST CONDITIONS:
Connector going to the Y-SUS P811 is disconnected.
P500 on the Main board disconnected (coming in on P813).
Use the holes on the connector P500 (Main Board side) to insert the resistors and jumper lead.
Connect (2) 100 Watt light bulbs in series between VS and Ground.

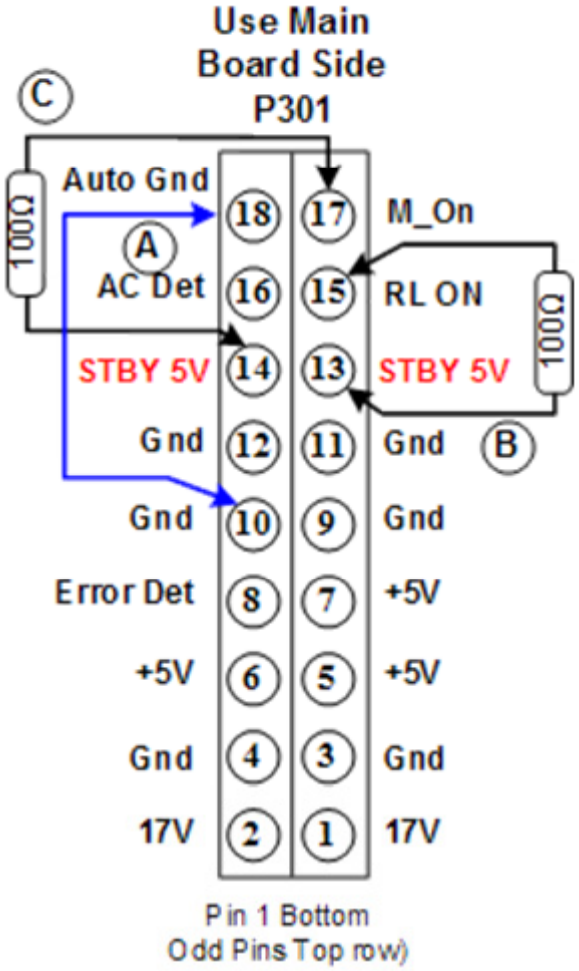
When the supply is operational in its normal state the Auto Ground line at Pin 18 of P813 is held at ground by the Main Board.
This Power Supply can be powered on sequentially to test the Controller Chip IC701 operational capabilities and for troubleshooting purposes.
By disconnecting P500, pin 18 is opened. To return the SMPS to the normal state for this test procedure, this pin must be grounded.
(See first step A below).

Note: Leave previous installed 100Ω resistor in place when adding the next resistor.

(A) Ground the Auto Gnd Line (Pin 18) will allow the supply to be powered up one section at a time.

(B) Add a 100Ω ¼ watt resistor from 5V Standby to RL_ON and the 17V and 5V Run Lines on P813 will become active. Also AC-Det (4.06V) and Error_Det (4.1V) become active (Not Used).

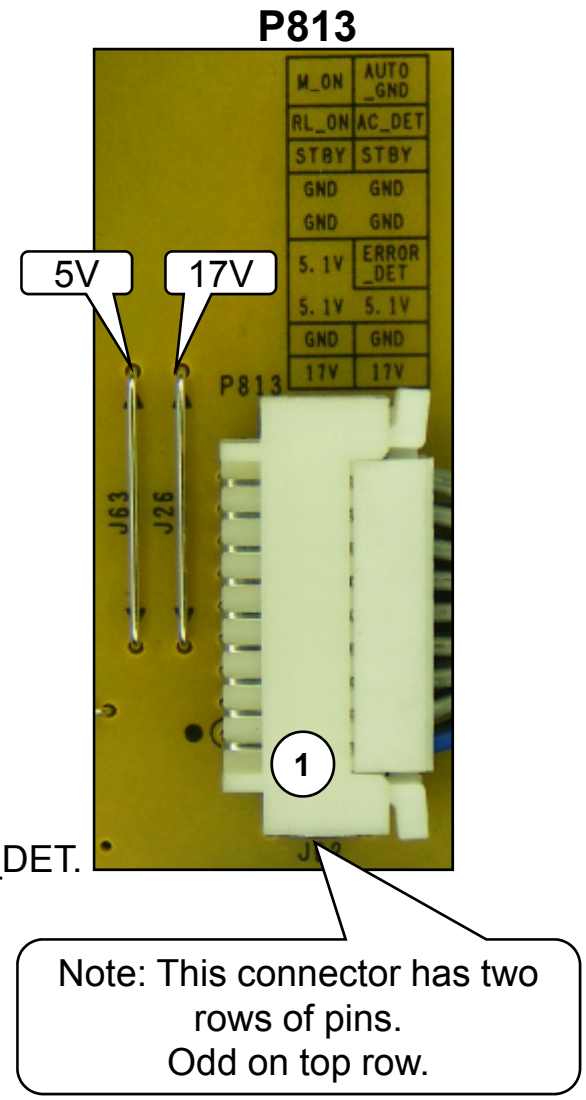
(C) Add a 100Ω ¼ watt resistor from any 5V line to M_ON to make the (Monitor) M5V, VS and VA lines operational.
P811 (VS pins 1 and 2) and (VA pins 6).
P811 (M5V pin 7)



P813 SMPS Connector Identification, Voltages and Diode Check

P813 Connector "SMPS" to "Main" P500

Pin	Label	STBY	Run	No Load	Diode
18	[e]Auto_Gnd	Gnd	Gnd	4.86V	Open
17	[b]M_ON	0V	3.28V	0V	Open
16	[a d]AC Det	0V	4.06V	4.94V	3.1V
15	[a]RL_ON	0V	3.28V	0V	Open
13-14	STBY_5V	3.47V	5.14V	4.94V	2.53V
9-12	Gnd	Gnd	Gnd	Gnd	Gnd
8	[a c]Error_Det	3.44V	4.02V	4.94V	2.84V
5-7	[a]5.1V	0.46V	5.17V	5.22V	2.13V
3-4	Gnd	Gnd	Gnd	Gnd	Gnd
1_2	[a]17V	0V	17V	17V	3.06V



a Note: The RL_On command turns on the 17V, +5V, Error_Det and AC_DET.
b Note: The M-On command turns on M5V, Va and Vs.
c Note: The Error Det line is not used in this model.
d Note: AC Det if missing, the TV will attempt to turn on, but shut off.
e Note: Pin 18 is grounded on the Main. If opened, the power supply turns on automatically.

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P811 and SC101 SMPS Connector Identification, Voltages and Diode Check

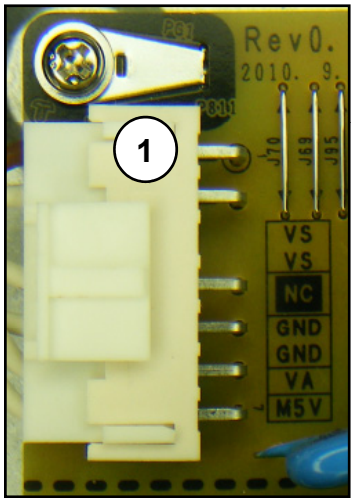
SC101 AC INPUT

Connector	Pin Number	Standby	Run	Diode Mode
SC101	L and N	120VAC	120VAC	Open

P811 "Power Supply“ to Y-SUS “P210”

Pin	Label	Run	Diode Check
1~2	Vs	*201V	Open
3	n/c	n/c	n/c
4~5	Gnd	Gnd	Gnd
6	Va	*55V	Open
7	M5V	5.0V	1.38V

P811



*** Note: This voltage will vary in accordance with Panel Label**

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

Y-SUS BOARD SECTION (Overview)

Y-SUS Board develops the Y-Scan drive signal to the Y-Drive boards.

This Section of the Presentation will cover alignment and troubleshooting the Y-SUS Board. Upon completion of the Section the technician will have a better understanding of the operation of the circuit and will be able to locate test points needed for troubleshooting and alignments.

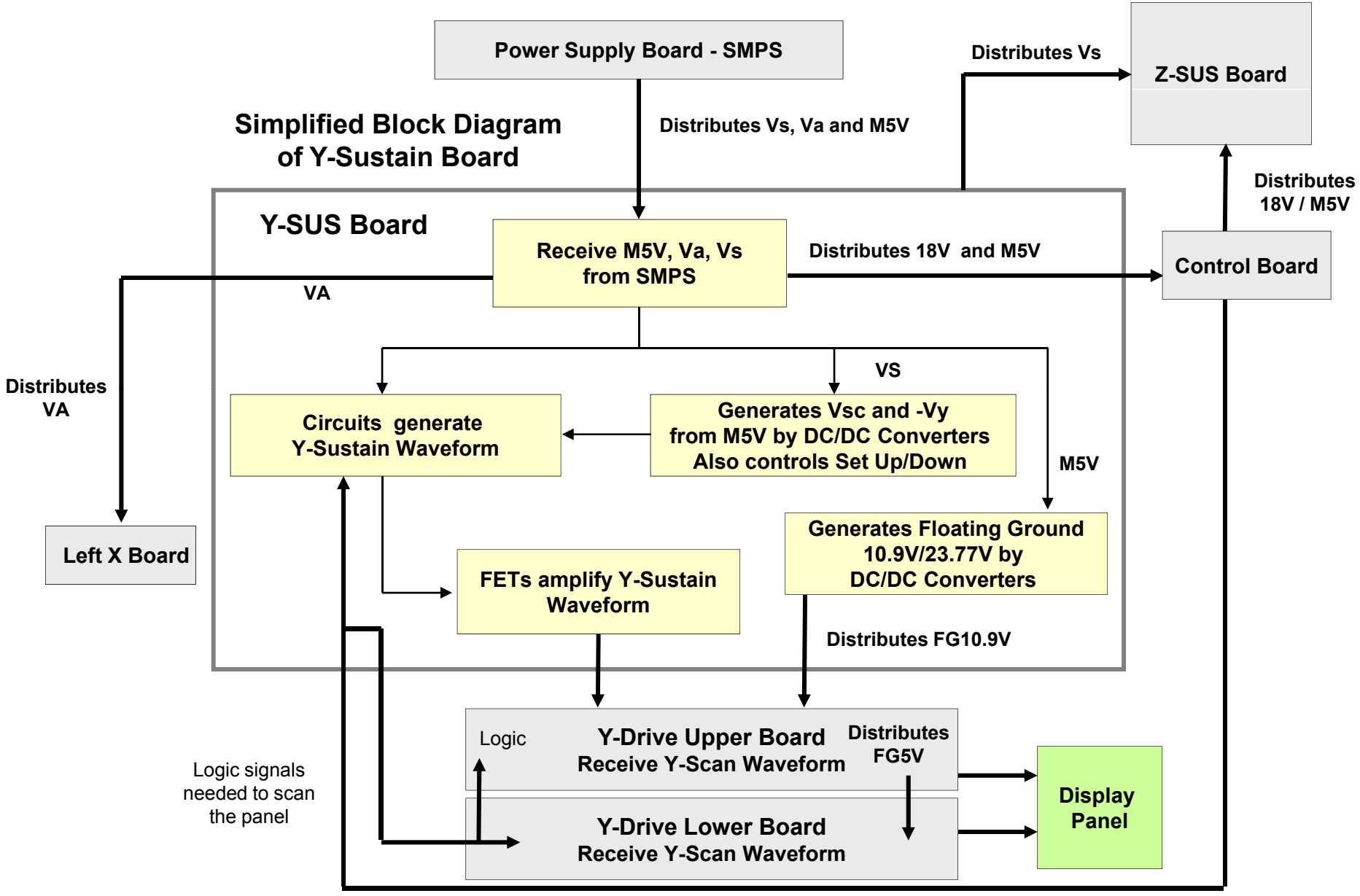
- Adjustments
- DC Voltage and Waveform Checks
- Diode Mode Measurements

Operating Voltages

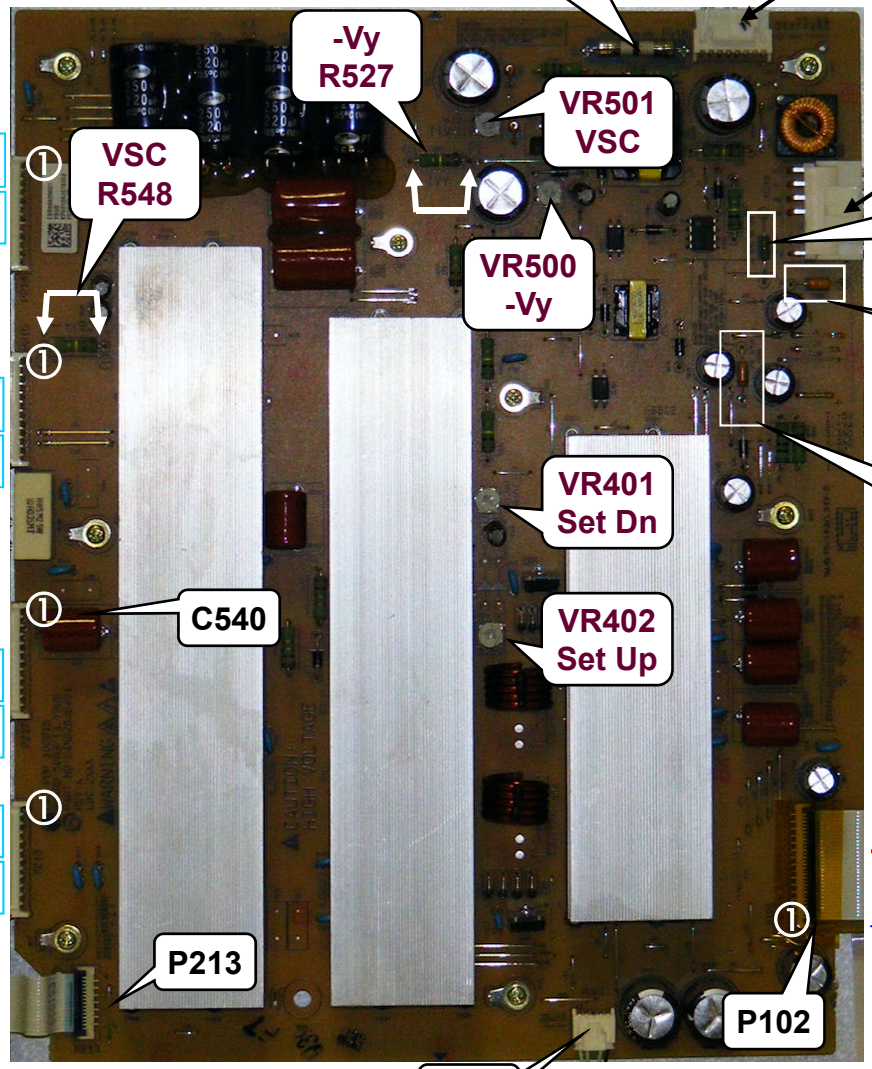
SMPS Supplied	VA	VA supplies the Panel's Vertical Electrodes (Routed to the Left X-Board)
	VS	VS Supplies the Panel's Horizontal Electrodes. Also routed out to the Z-SUS
	M5V	M5V Supplies Bias to Y-SUS. (From Y-SUS routed to the Control Board then Z-SUS). Also, in this set, M5V is routed to the Lower Y-Drive for the data buffers.
Y-SUS Developed	-VY VR501	-VY Sets the Negative excursion of Reset in the Drive Waveform
	VSC VR500	VSC Sets the amplitude of the complex waveform.
	V SET UP VR402	SET UP sets amplitude of the Top Ramp of Reset in the Drive Waveform
	V SET DN VR401	SET DOWN sets the Pitch of the Bottom Ramp for Reset in the Waveform
	18V	Used internally to develop the Y-Scan signal. (Also routed to the Control Board then routed to the Z-SUS board).
Floating Ground	FG 10.9V	Used on the Y-Drive boards (Measured from Floating Gnd)
	FG 23.77V	Used in the Development of the Drive Waveform (Measured from Floating Gnd)

-Vy and VSC generated when Vs arrives on the board. FG10.9V, FG23.77V and 18V generated when M5V arrives on the board.

Y-SUS Block Diagram



Y-SUS Board Layout



FS203 (VS)
6.3A/250V

P218 To Z-SUS

VS, VA and M5V
Input from the SMPS

-Vy
R527

VR501
VSC

VSC
R548

VR500
-Vy

P210

FS202 (M5V)
10A/125V

FS201 (VA)
4A/125V

FS501 (18V)
2A/125V

FG10.9V Pins 1-2

P214 To Y-Drive Upper

P215 To Y-Drive Upper

Y-Scan Pins 9~12

Or use the
Left Side
of C540

VR401
Set Dn

C540

VR402
Set Up

Y-Scan Pins 1~4

P217 To Y-Drive Lower

Y-Scan Pins 11~12

P216 To Y-Drive Lower

18V (pins 6~8)
to Control for Z-SUS
M5V (pins 3~5)

Ribbon

Logic Signals from
the Control Board

P213

P102

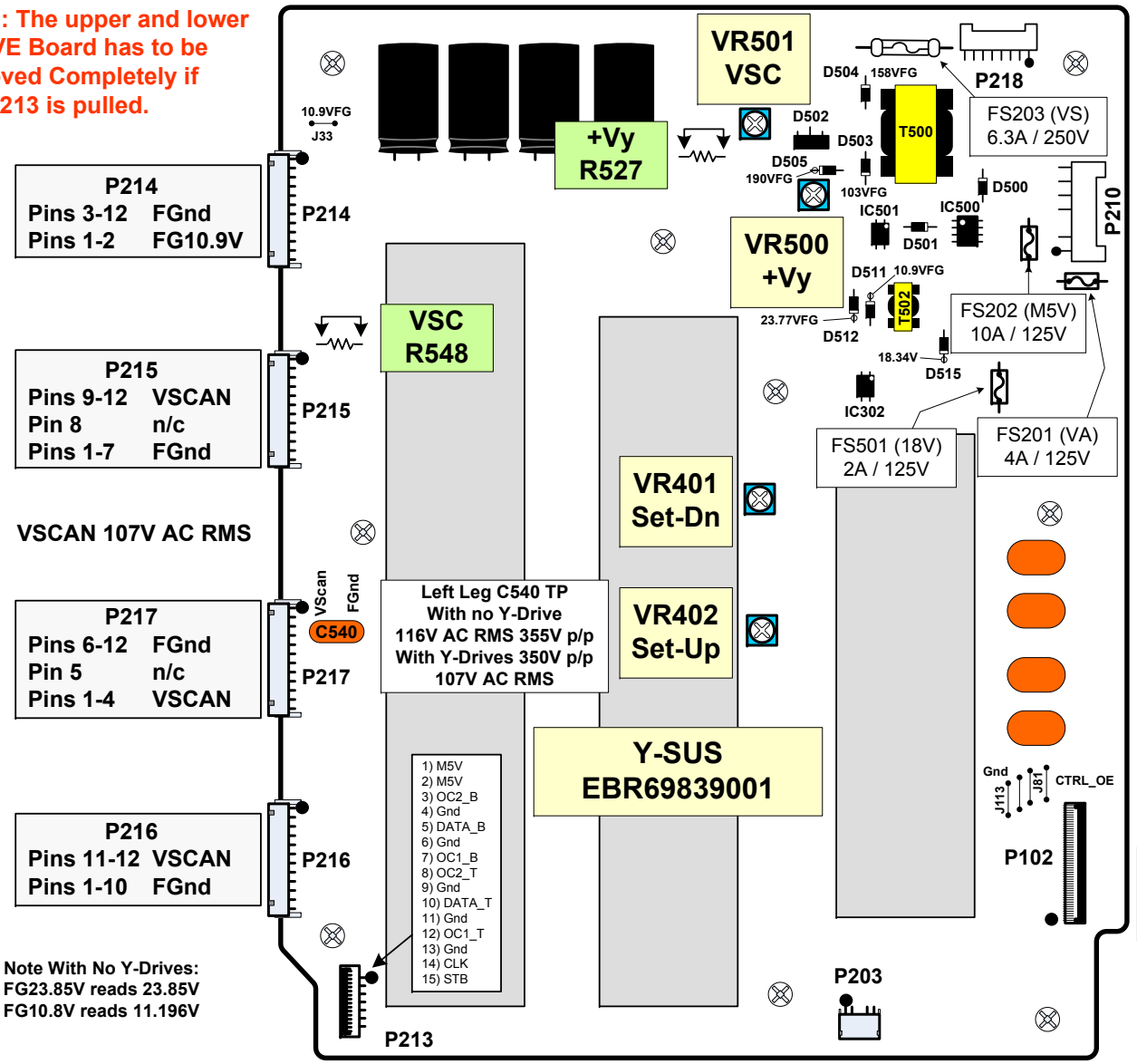
P203

Va to Left X Board
Pins 5~7

WARNING: Do not run set if P213
is removed. Damage will occur.

50PZ950 Y-SUS Board Component Layout

WARNING: The upper and lower Y-DRIVE Board has to be Removed Completely if P213 is pulled.



P214
Pins 3-12 FGnd
Pins 1-2 FG10.9V

P215
Pins 9-12 VSCAN
Pin 8 n/c
Pins 1-7 FGnd

VSCAN 107V AC RMS

P217
Pins 6-12 FGnd
Pin 5 n/c
Pins 1-4 VSCAN

P216
Pins 11-12 VSCAN
Pins 1-10 FGnd

Note With No Y-Drives:
FG23.85V reads 23.85V
FG10.8V reads 11.196V

To run the 18V and Floating Ground 24V and 10V, Ground CTRL_OE and supply 5V to Y-SUS

P203
1-2) Gnd
3) n/c
4-5) VA

P218
7-8) Gnd
6) n/c
4-5) VS
3) n/c
1-2) ER

P210
7) M5V
6) VA
4-5) Gnd
3) n/c
1-2) VS

D512 23.77VFG Diode Check
3.1V Red lead on FG
Open Blk lead on FG

D511 10.9VFG Diode Check
0.55V Red lead on FG
Open Blk lead on FG

FS201 Va or FS203 Vs Diode Check reads Open with Board Disconnected or Connected

FS202 M5V Diode Check reads 0.73V Board Connected or 1.38V Disconnected

FS501 Protects 18V Creation D515 and T502 Diode Check With Board 1.28V Connected or 1.31V Disconnected

Example:

Model : PDP 50R3###
Voltage Setting: 5V/ Va:55/ Vs:201
N.A. / -190 / 150 / N.A. / 130
Max Watt : 360 W (Full White)

-Vy VSC

CTRL_OE should be 0V (5V indicates and problem)

P102
6-8) 18V
3-5) M5V

P213 to P213	RUN	DIODE
1) M5V	4.96V	1.38V
2) M5V	4.96V	1.38V
3) OC2_B	2.77V	Open
4) Gnd	Gnd	Gnd
5) DATA_B	0V	1.85V
6) Gnd	Gnd	Gnd
7) OC_B	1.73V	1.85V
8) OC2_T	2.73V	Open
9) Gnd	Gnd	Gnd
10) DATA_T	0V	1.85V
11) Gnd	Gnd	Gnd
12) OC1_T	1.74V	1.85V
13) Gnd	Gnd	Gnd
14) CLK	0.68V	1.85V
15) STB	4.27V	1.85V

Referenced to Chassis Gnd

VSC and -VY Adjustments

CAUTION: Use the actual panel label and not the book for exact voltage settings.

These are DC level Voltage Adjustments

Set should run for 10 minutes, this is the "Heat Run" mode.
Set screen to "White Wash".
1) Adjust –Vy (VR500) to Panel's Label voltage (+/- 1/2V)
2) Adjust VSC (VR501) to Panel's Label voltage (+/- 1/2V)

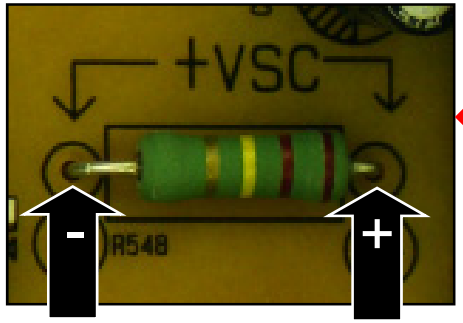
This is just for example

Model : PDP 50R3###
Voltage Setting: 5V/ Va:55/ Vs:201
N.A. / -190 / 150 / N.A. / 130
Max Watt : 360 W (Full White)

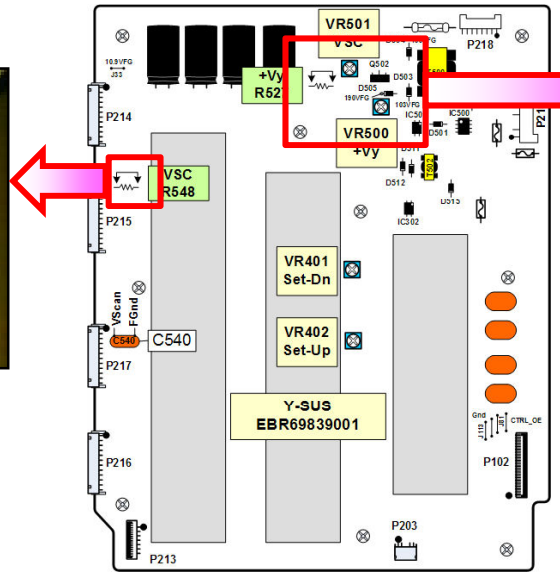
-Vy ***VSC***

Voltage Reads Positive

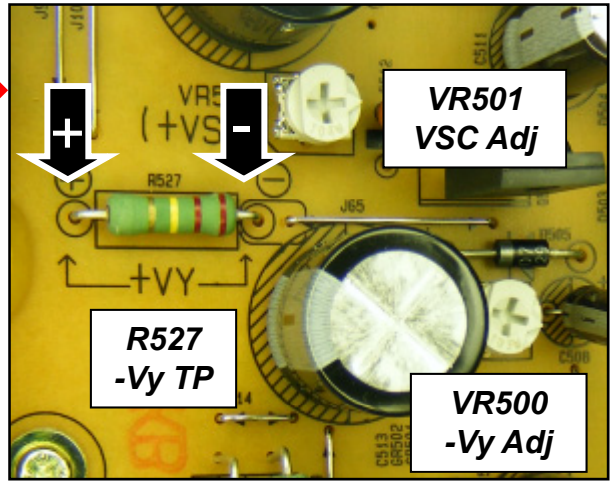
R548
VSC TP



Location:
Center Top
Left of board



-Vy Voltages Reads Positive



Location: Top Right
of board

Y-Scan Signal Overview

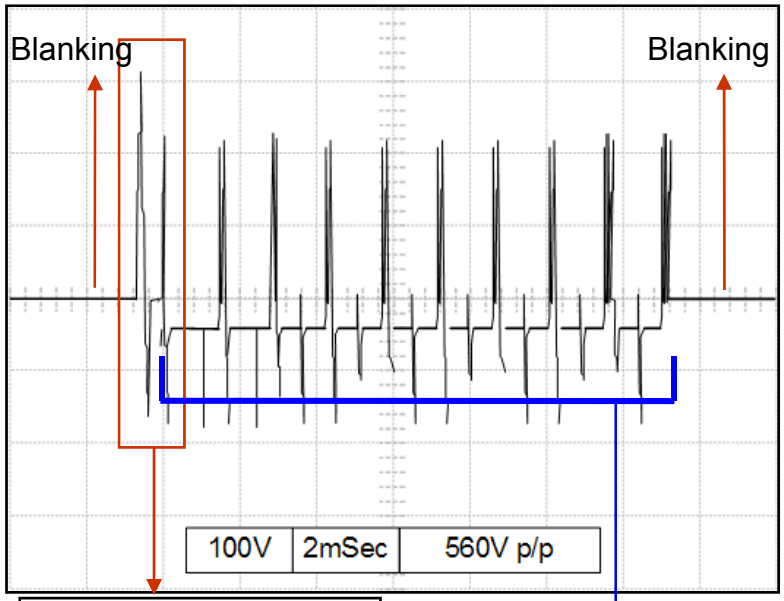
Y-Drive Upper Test Point
Just above 2nd Buffer from bottom

NOTE: The Waveform Test Points are fragile. If by accident the land is torn and the run lifted, make sure there are no lines left to right in the screen picture.

There is another test point on the Upper Y-Drive board that can be used.
Basically any output pin to any of the FPC to the panel are OK to use.

Overall signal observed 2mS/div

107VRMS **560V p/p**



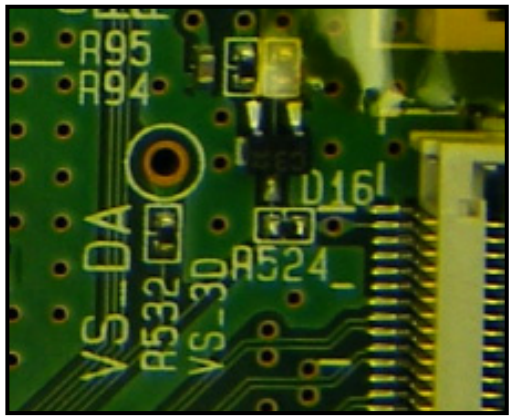
Adjustment Area

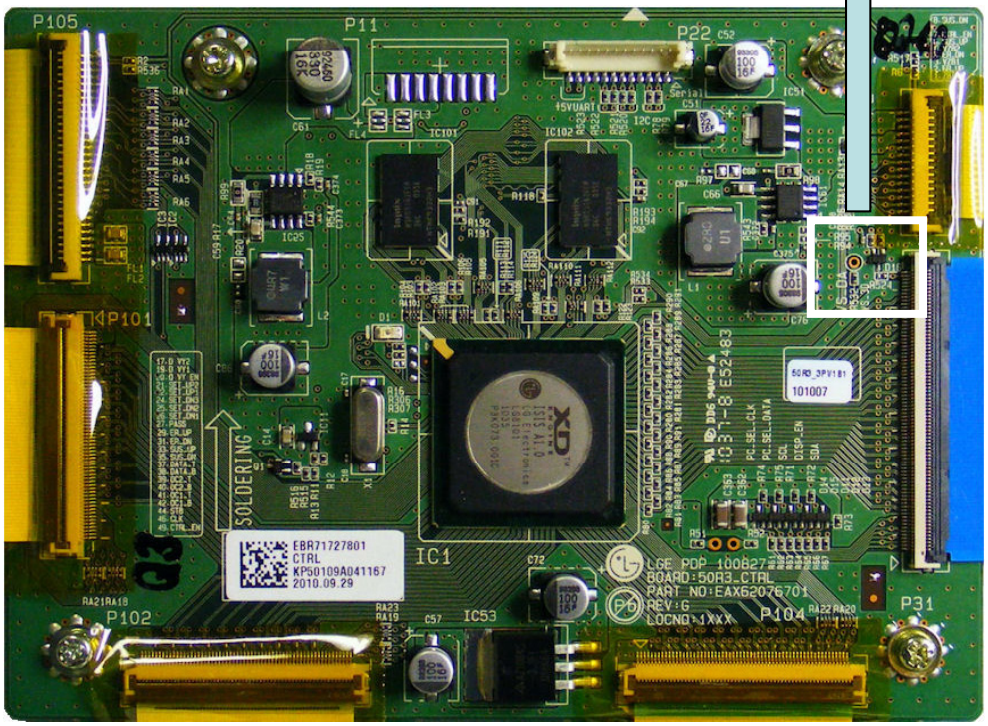
X10 Sub Field Firing
(600Hz)
Video

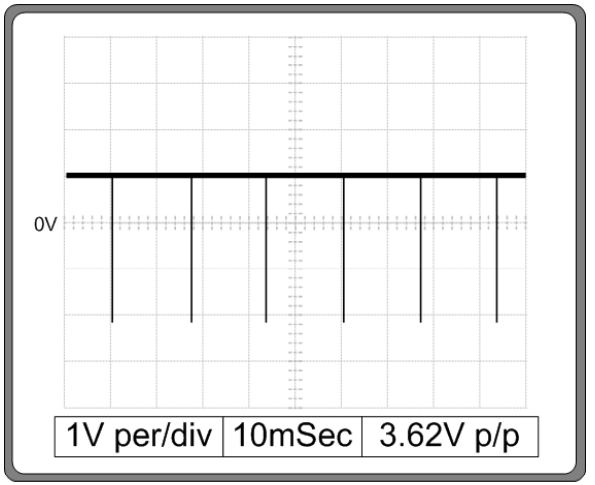
Locking on to the Y-Scan Waveform Tip

Note, this TP (VS_DA) can be used as an External Trigger for scope when locking onto the Y-Scan (Scan) or the Z-Drive signal.

This signal can also be used to help lock the scope when observing the LVDS video signals.







Observing (Capturing) the Y-Scan Signal for Set Up Adjustment

Set must be in "WHITE WASH"
All other DC Voltage adjustments should have already been made.

Fig 1:
As an example of how to lock in to the Y-Scan Waveform. Fig 1 shows the signal locked in at 4ms per/div.
Note the 3 blanking sections.
The area for adjustment is pointed out within the Waveform

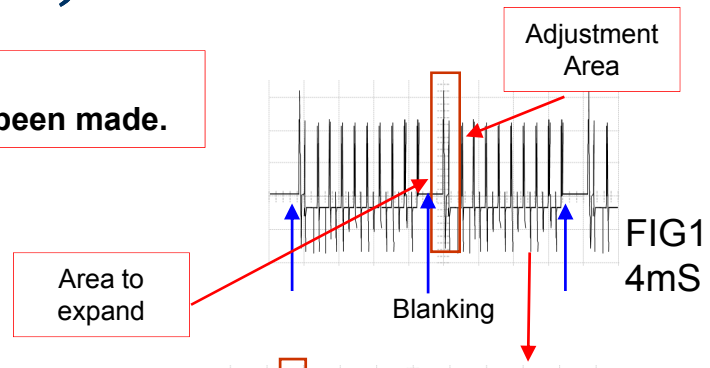


FIG1
4mS

Fig 2:
At 2mSec per/division, the area of the waveform to use for **SET-UP** or **SET-DN** is now becoming clear.
Now only two blanking signals are present.

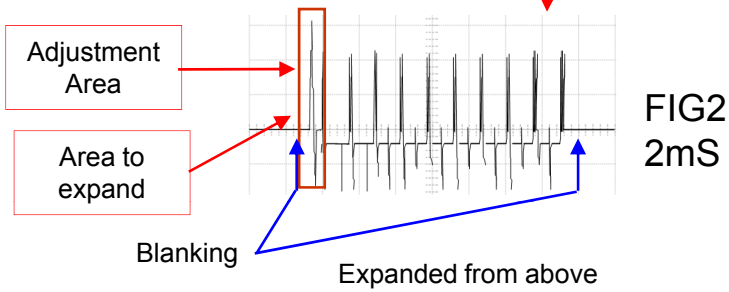


FIG2
2mS

Fig 3:
At 100us per/div the area for adjustment of **SET-UP** or **SET-DN** is now easier to recognize. It is outlined within the Waveform.
Remember, this is the 1st large signal to the right of blanking.

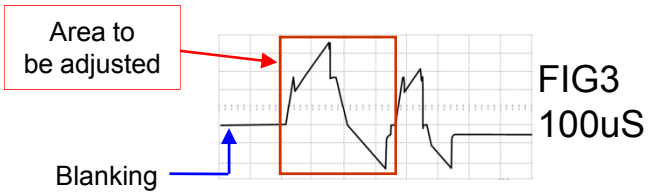


FIG3
100uS

Fig 4:
At 40uSec per/division, the adjustment for **SET-UP** can be made using **VR402** and the **SET-DN** can be made using **VR401**.
It will make this adjustment easier if you use the "Expanded" mode of your scope.

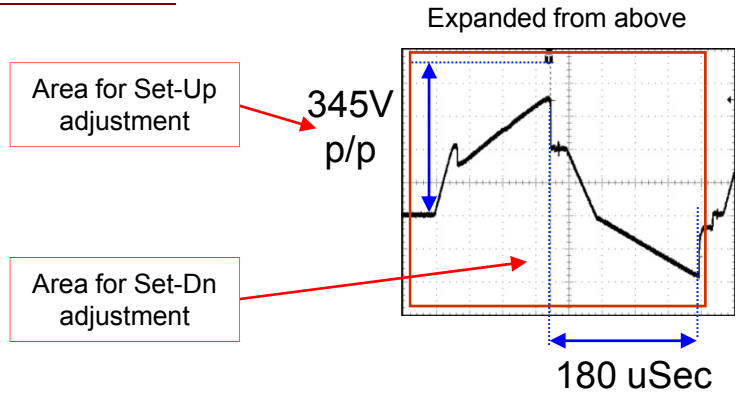


FIG4
40uS

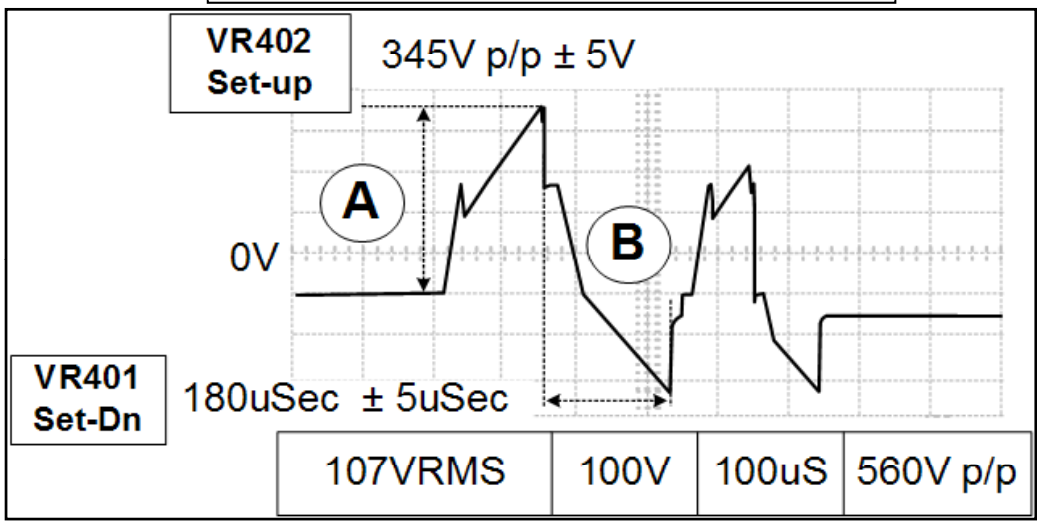
Set Up and Set Down Adjustments

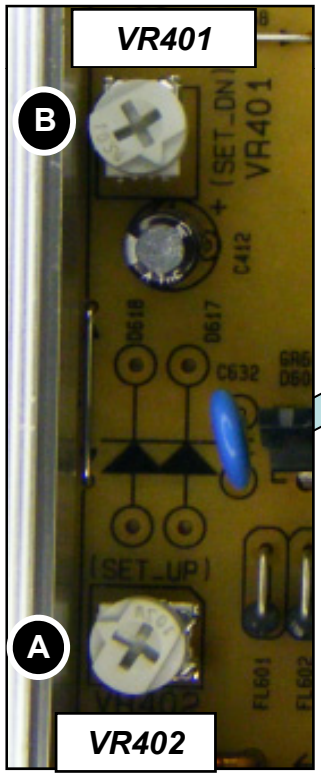
Y-Scan Test Point

Upper Y-Drive

Set must be in "WHITE WASH"
All other DC Voltage adjustments should have already been made.

Waveform Test Point
Y-Drive Upper or Lower (Waveform TP)





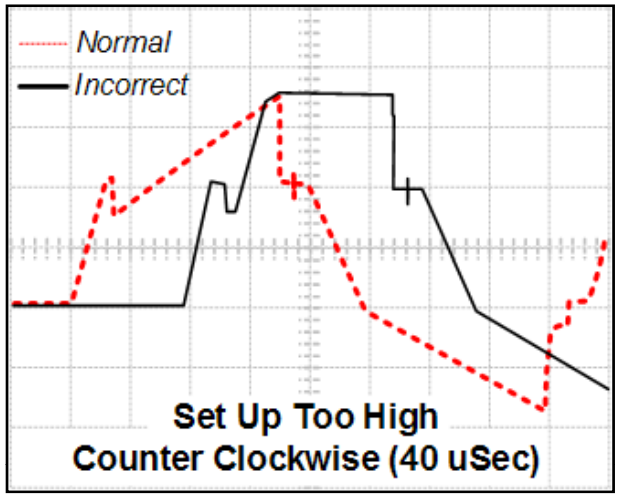
ADJUSTMENT LOCATIONS: Center of the board.

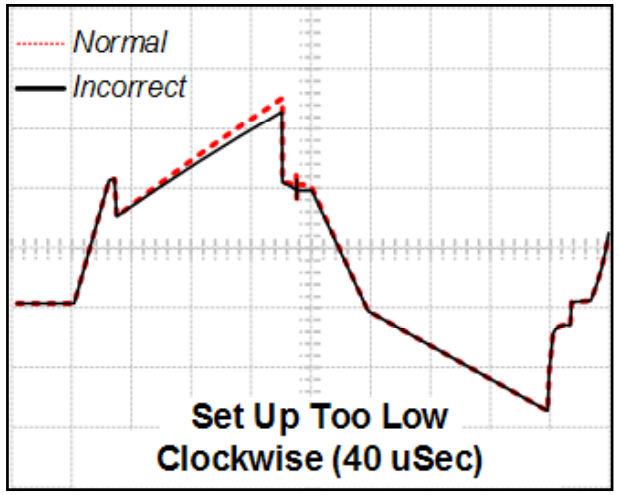
SET-UP ADJUST:
1) Adjust **VR402** and set the **(A)** portion of the signal to match the waveform above. (345V p/p ± 5V)

SET-DN ADJUST:
2) Adjust **VR401** and set the **(B)** time of the signal to match the waveform above. (180uSec ± 5uSec)

Set Up/Down Adjustments Too High or Low

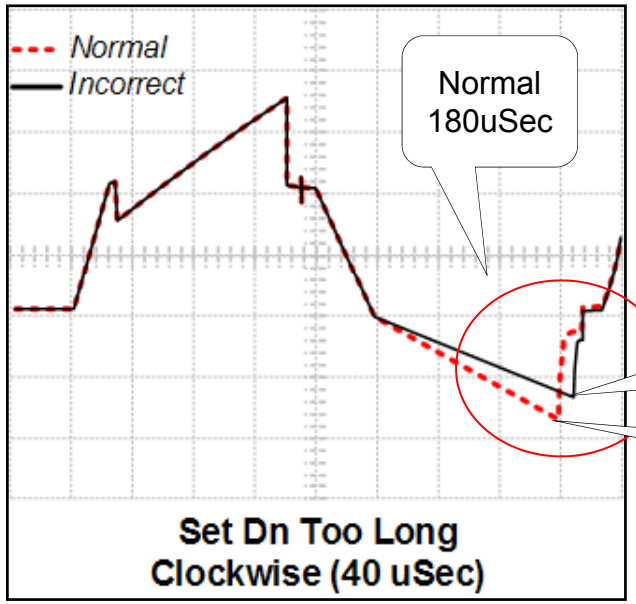
Set Up swing is Minimum 328V p/p Max 358V p/p





This will cause
The black
Portions of the
Picture to
Lighten.
Black floor Up.

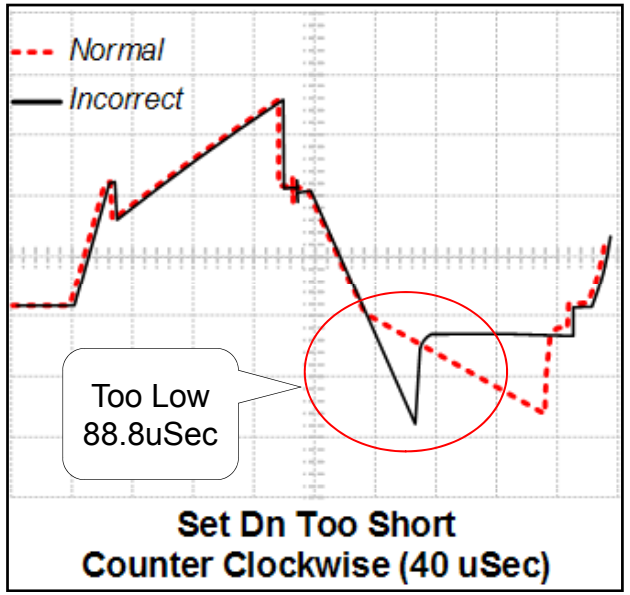
Set Dn swing is Minimum 73uSec Max 196uSec



This will cause
The bottom of
The picture to distort.

40V off the
Floor

Floor



NOTE: If abnormal settings cause excessive brightness then shutdown, remove the LVDS from Control board and make necessary adjustments. Then reconnect LVDS cable, select White Wash and adjust correctly.

Y-SUS Board Troubleshooting Y-Drive

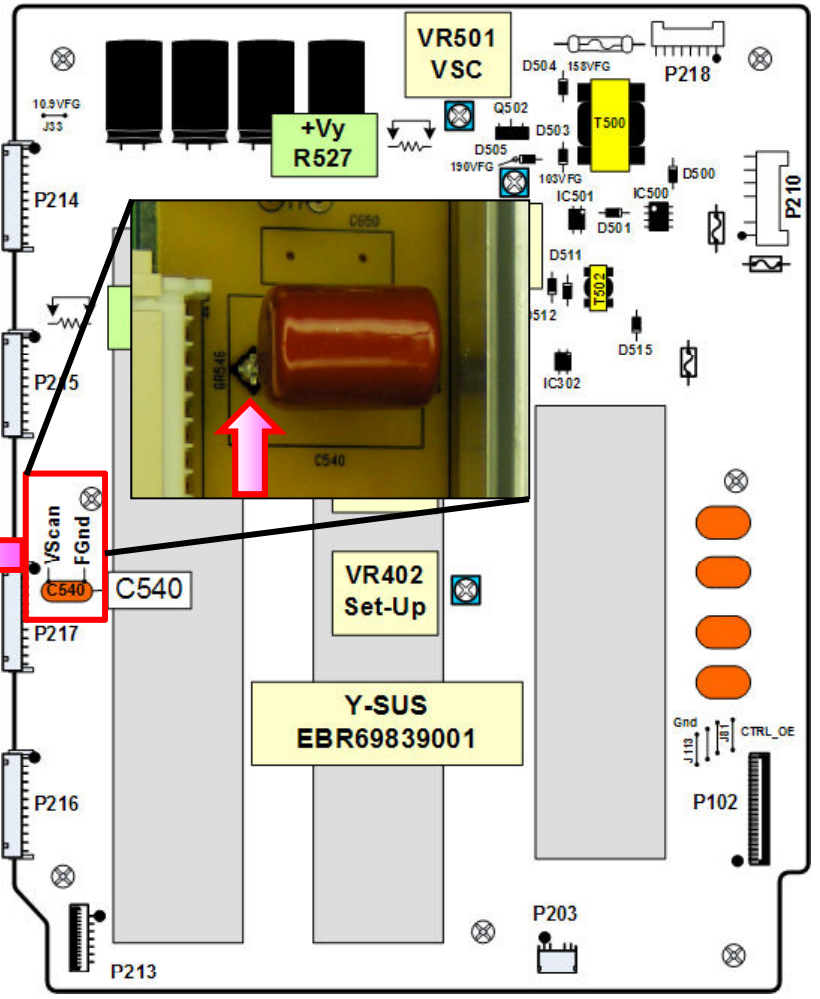
Y-SUS Board develops the Y-Scan drive signal to the Y-Drive boards.

This Section of the Presentation will cover troubleshooting the Y-SUS Board.

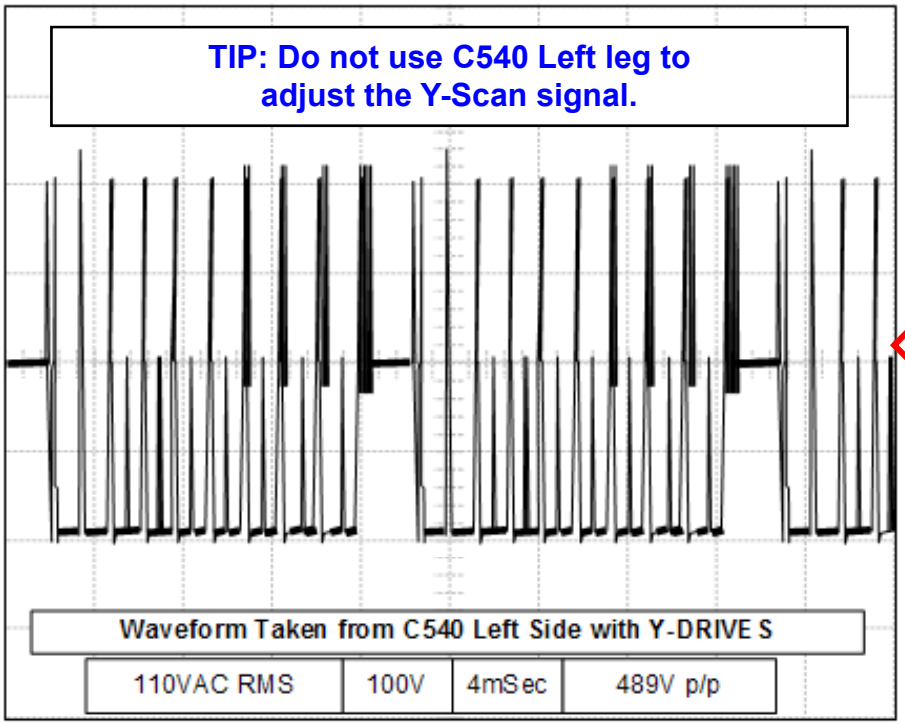
Warning: Never run the Y-SUS with P213 removed unless the Y-Drive boards are removed completely. The same is true for P221/P121 and the Upper Y-Drive.

TIP: Use C540 Left leg to check the Y-Scan signal if the Y-Drive boards are removed

P/N EBR69839001



TIP: Do not use C540 Left leg to adjust the Y-Scan signal.



Waveform Taken from C540 Left Side with Y-DRIVE S			
110VAC RMS	100V	4mSec	489V p/p

WITH NO Y-DRIVE S (Remove the boards first)			
127.7VAC RMS	100V	4mSec	424V p/p

P102 Y-SUS Board Ribbon to Control P203 Voltage and Diode Test

P102 "Y-SUS" to P105 "Control"

Pin	Label	Run	Diode Check
30	CTRL_OE	0.06V	Open
29	OE	0.02V	2.29V
28	SUS_UP	0.13V	Open
27	SUS_DN	2.84V	Open
26	SET_DN	2.2V	Open
25	Slope_Rate_Sel	0.05V	Open
24	Det_Level_Sel	0.3V	Open
23	Ramp_Slope_Opt1	0.06V	Open
22	SET_UP	0.06V	Open
21	YER_UP	0.11V	Open
20	Gnd	Gnd	Gnd
19	YER_DN	0.09V	Open
18	PASS_TOP	1.02V	Open
17	DELTA_VY_DET	0.35V	Open
16	OC2_TOP	1.98V	Open

Pin	Label	Run	Diode Check
15	DATA_TOP	0V	Open
14	OC1_TOP	1.16V	Open
13	CLK	0.46V	Open
12	STB	2.86V	Open
11	OC1_BTM	Gnd	Open
10	DATA_BTM	0V	Open
9	OC2_BTM	1.98V	Open
8	**+18V**	**18.34V**	**1.32V**
7	**+18V**	**18.34V**	**1.32V**
6	**+18V**	**18.34V**	**1.32V**
5	**M5V**	**4.89V**	**1.40V**
4	**M5V**	**4.89V**	**1.40V**
3	**M5V**	**4.89V**	**1.40V**
2	Gnd	Gnd	Gnd
1	Gnd	Gnd	Gnd

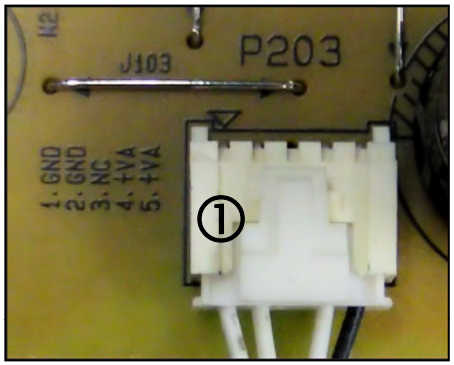
Location: Bottom Right of board

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P203 Y-SUS Board to Left X-Board P121 Voltage and Diode Test

Location: Bottom Right of board

P203



To Left X-Board

P203 "Y-SUS" to "X-Drive Left" P121

Pin	Label	Run	Diode Check
1~2	Gnd	Gnd	Gnd
3	n/c	n/c	Open
4~5	Va	*55V	Open

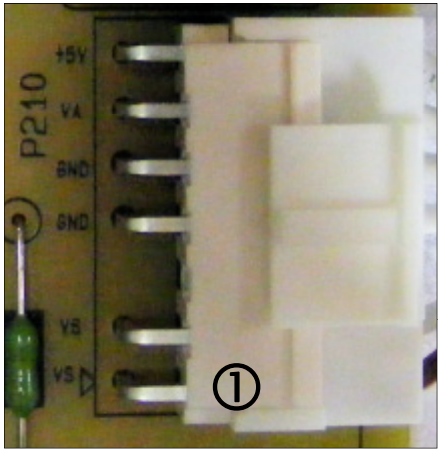
* Note: This voltage will vary in accordance with Panel Label

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P210 Y-SUS Board to SMPS P811 Voltage and Diode Test

Location: Top Right of board

P210



To SMPS

P210 "Y-SUS" to "Power Supply" P811

Pin	Label	Run	Diode Check
1~2	Vs	*201V	Open
3	n/c	n/c	n/c
4~5	Gnd	Gnd	Gnd
6	Va	*55V	Open
7	M5V	5.0V	1.38V

* Note: This voltage will vary in accordance with Panel Label

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

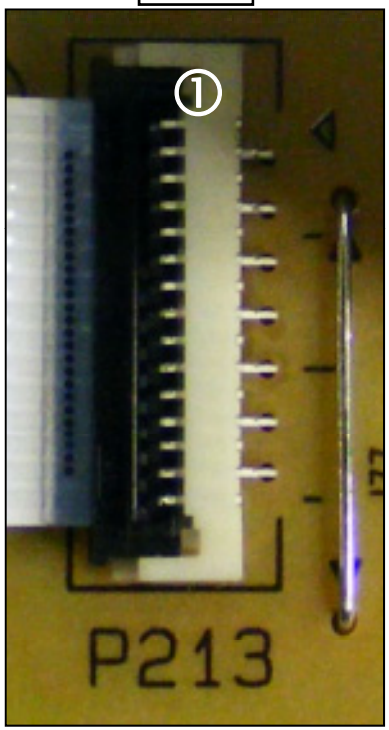
P213 Y-SUS Board Connector to P213 Lower Y-Drive (Logic Signals)

TIP: This connector does not come with a new Y-SUS or Y-Drive.

TIP: Use C540 Left leg to check the Y-Scan signal if the Y-Drive boards are removed

Note: The Lower Y-Drive board receives Monitor 5V from the Y-SUS.

P213



Y-SUS Board

P213 Y-SUS to Lower Y-Drive P213

Pin	Label	Run	Diode Check
1	**M5V**	**4.96V**	**1.38V**
2	**M5V**	**4.96V**	**1.38V**
3	OC2_B	2.77V	Open
4	Gnd	Gnd	Gnd
5	DATA_B	0V	1.85V
6	Gnd	Gnd	Gnd
7	OC1_B	1.73V	1.85V
8	OC2_T	2.73V	Open
9	Gnd	Gnd	Gnd
10	DATA_T	0V	1.85V
11	Gnd	Gnd	Gnd
12	OC1_T	1.74V	1.85V
13	Gnd	Gnd	Gnd
14	CLK	0.68V	1.85V
15	STB	4.27V	1.85V

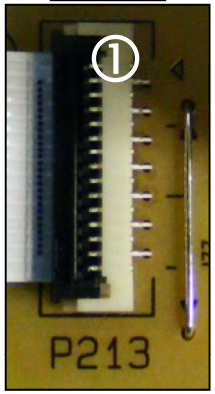
All readings taken from Chassis Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P213 Y-SUS Board Connector Waveforms

Note: The Lower Y-Drive board receives Monitor 5V from the Y-SUS.

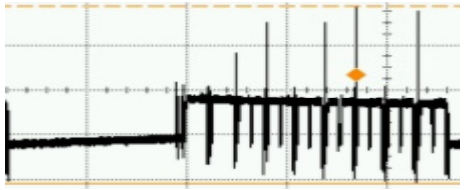
P213



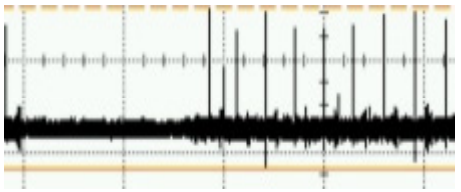
P213 Y-SUS to Lower Y-Drive P213

Pin	Label
1	M5V
2	M5V
3	OC2_B
4	Gnd
5	DATA_B
6	Gnd
7	OC1_B
8	OC2_T
9	Gnd
10	DATA_T
11	Gnd
12	OC1_T
13	Gnd
14	CLK
15	STB

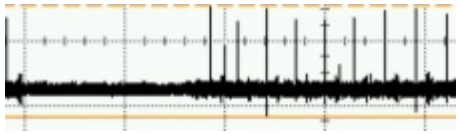
Pin 3 (19.9V p/p)



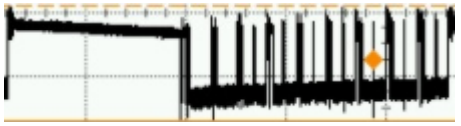
Pin 10 (8.47V p/p)



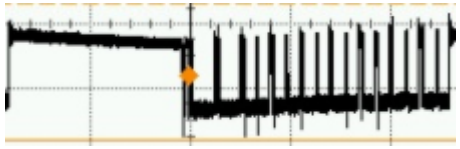
Pin 5 (8.62V p/p)



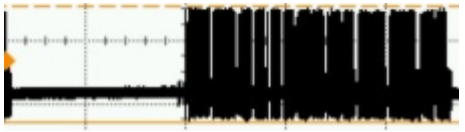
Pin 12 (9V p/p)



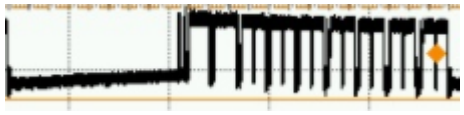
Pin 7 (10.67V p/p)



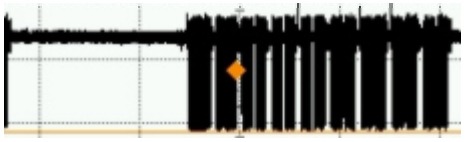
Pin 14 (9.08V p/p)



Pin 8 (10.67V p/p)



Pin 15 (11.15V p/p)

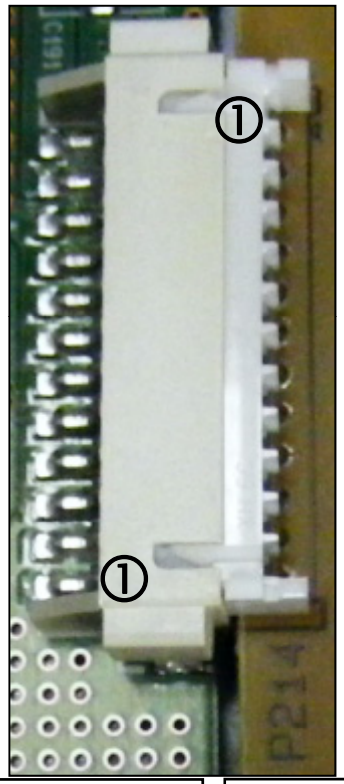


All scope settings at 5mSec per/div / 5V per/div
All signals taken from Chassis Ground

P214 Y-SUS Board to Upper Y-Drive P111 Voltage and Diode Test

Location: Top Left of board

P111 **P214**



Y-Drive Upper **Y-SUS Board**

P214 "Y-SUS" to "Upper Y-Drive" P111

Pin	Label	Run	Diode Check	Diode Check
3-12	FGnd	FGnd	FGnd	FGnd
1-2	FG10.9V	4.89V	Open	0.55V
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

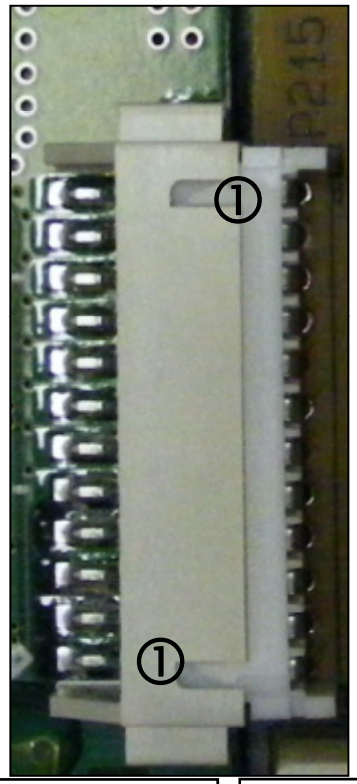
All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P215 Y-SUS Board to Upper Y-Drive P112 Voltage and Diode Test

Location: Bottom Left of board

P112 **P215**



Y-Drive Upper **Y-SUS Board**

P215 "Y-SUS" to "Upper Y-Drive" P112

Pin	Label	Run	Diode Check	Diode Check
9-12	Vscan	107V	Open	Open
8	n/c	n/c	n/c	n/c
1-7	FGnd	FGnd	FGnd	FGnd
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

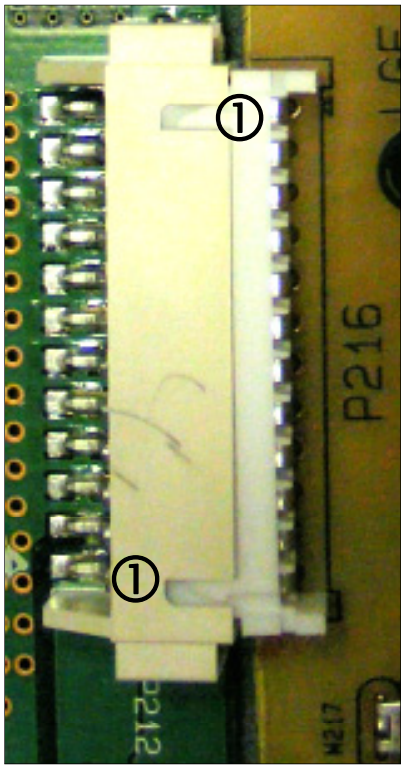
All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P216 Y-SUS Board to Lower Y-Drive P212 Voltage and Diode Test

Location: Bottom Left of board

P212 **P216**



Y-Drive Upper **Y-SUS Board**

P216 "Y-SUS" to "Lower Y-Drive" P212

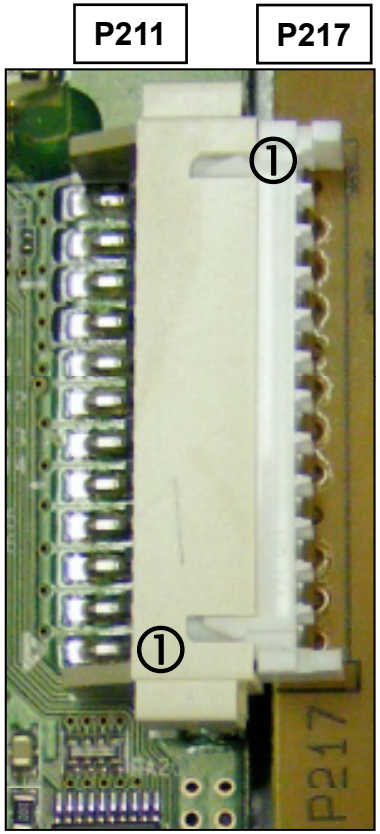
Pin	Label	Run	Diode Check	Diode Check
11-12	Vscan	107V	Open	Open
1-10	FGnd	FGnd	FGnd	FGnd
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P217 Y-SUS Board to Lower Y-Drive P211 Voltage and Diode Test

Location: Bottom Left of board



Y-Drive Upper **Y-SUS Board**

P217 "Y-SUS" to "Lower Y-Drive" P211

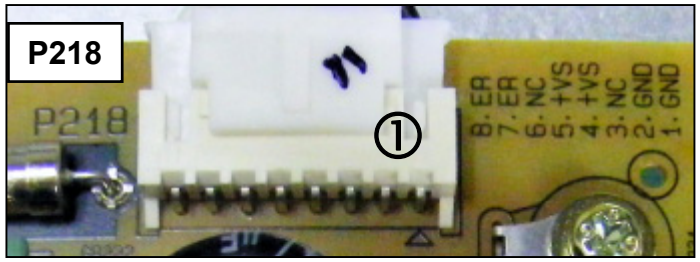
Pin	Label	Run	Diode Check	Diode Check
6-12	FGnd	FGnd	FGnd	FGnd
5	n/c	n/c	n/c	n/c
1-4	Vscan	107V	Open	Open
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

Y-SUS Board P218 to Z-SUS P203 Voltage and Diode Test

Location: Top Right of board



P218 "Y-SUS" to "Z-SUS" P203

Pin	Label	Run	Diode Check
1~2	Gnd	Gnd	Gnd
3	n/c	n/c	n/c
4~5	+Vs	*201V	Open
6	n/c	n/c	n/c
7~8	ER_PASS	*98V~102V	Open

* Note: This voltage will vary in accordance with Panel Label

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

Y-SUS Floating Ground FG10.9V, FG23.77V and 18V Checks

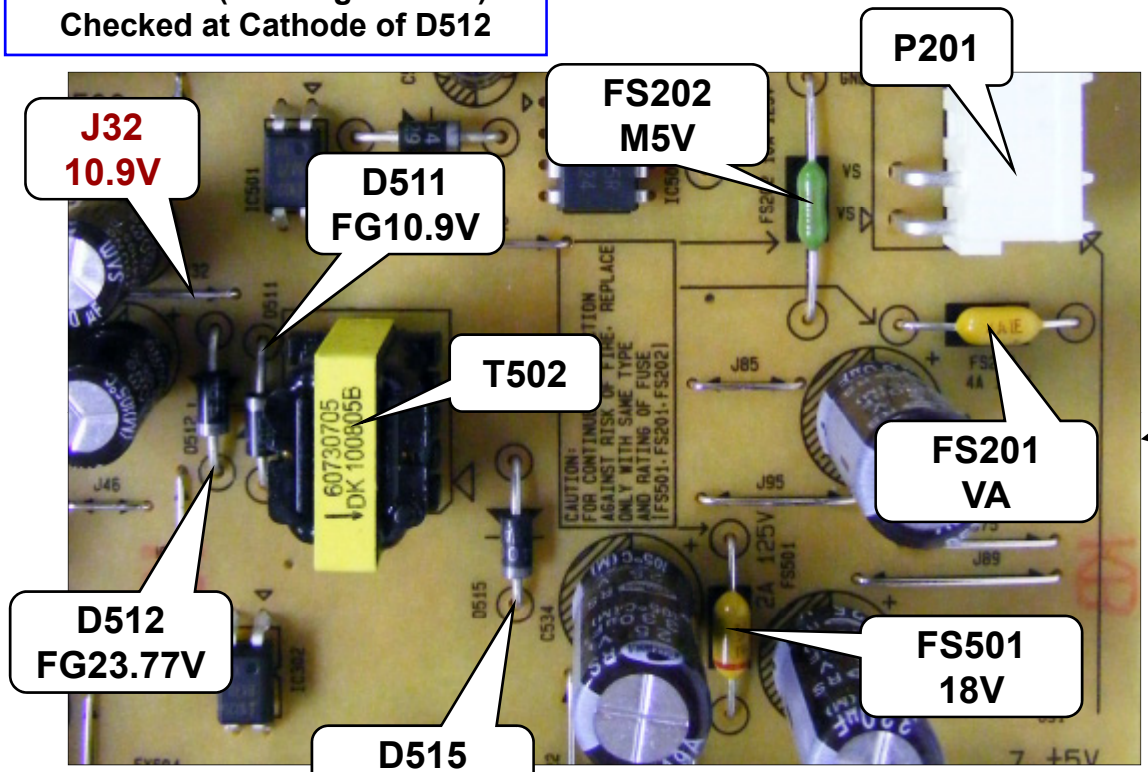
Voltage Measurements for the Y-SUS Board

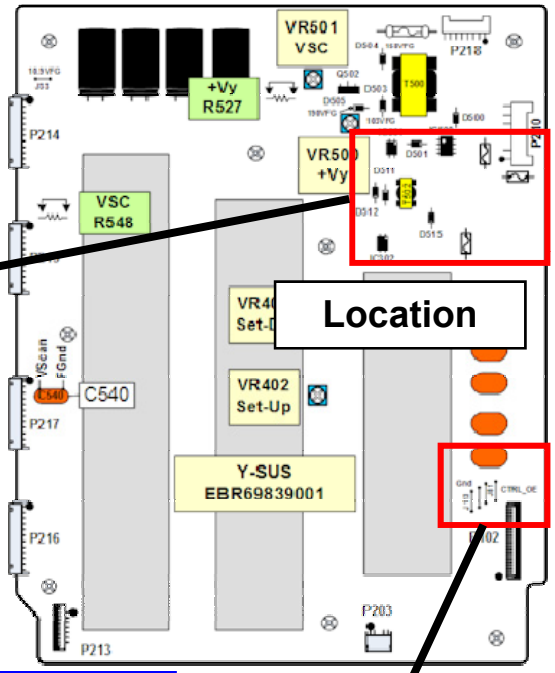
Floating Ground checks must be measured from Floating Ground. Use pins 3~12 on P214

Note With No Y-Drives:
FG23.77V reads 23.85VFG
FG10.9V reads 11.2VFG

FG23.77V (Floating Ground). Checked at Cathode of D512

Tip: M5V turns on these supplies.





FG10.9V (Floating Ground). Checked at Cathode of D511. Leaves the Y-SUS board to Upper Y-Drive on P214 pins 1 and 2

18V (Chassis Ground). Checked at Cathode of D515. Leaves the Y-SUS board to Control board on P102 pins 6~8

J81 (CTRL_OE)

Tip: Remove board, Ground J81 (CTRL_OE) Jump any 5V supply to pin 7 of P210 or FS202 and it will turn on these supplies for test.

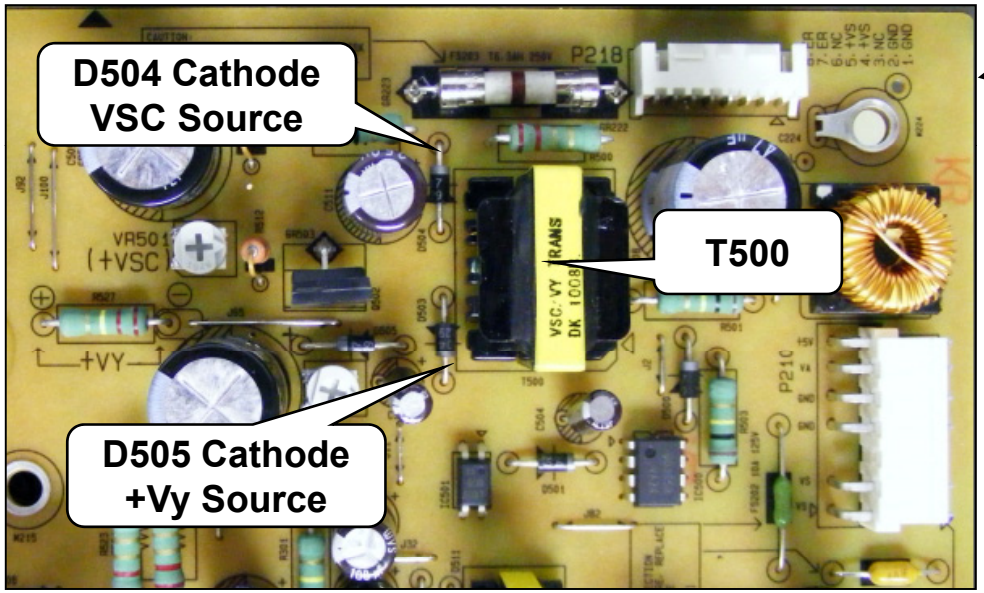
Y-SUS (VSC and –Vy) Generation Checks

Voltage Measurements for the Y-SUS Board

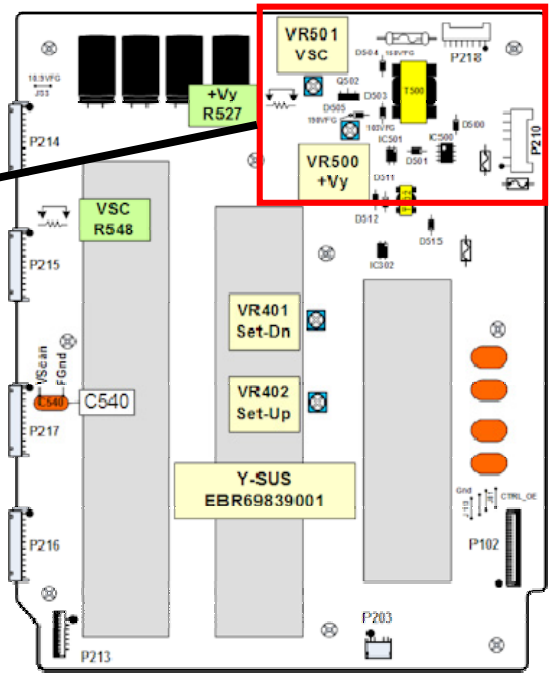
Tip: VS turns on these supplies, but Floating Gnd 10.9V, 23.77V and Chassis Gnd 18V must be running.

VSC Source Test Point. Used Y-SUS Waveform development. Checked at Cathode Side of D504.

Run: 158V Diode check: Open (Black lead on FGnd)
0.49V (Red lead on FGnd)



Location

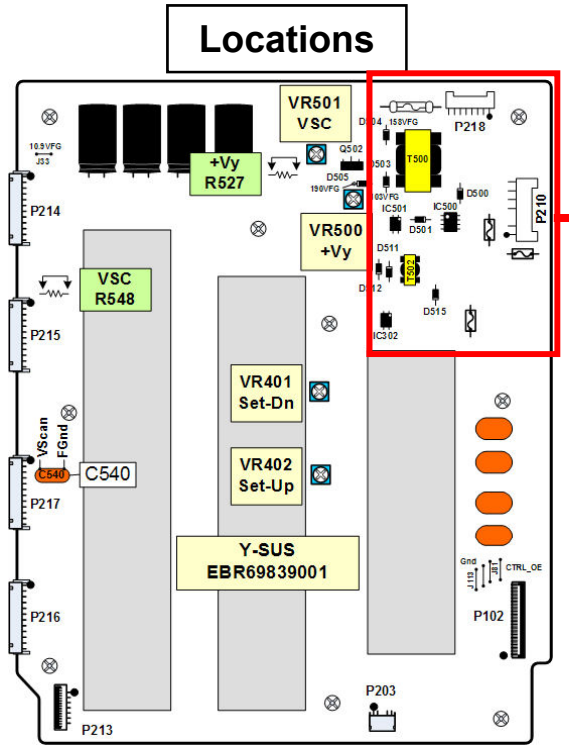


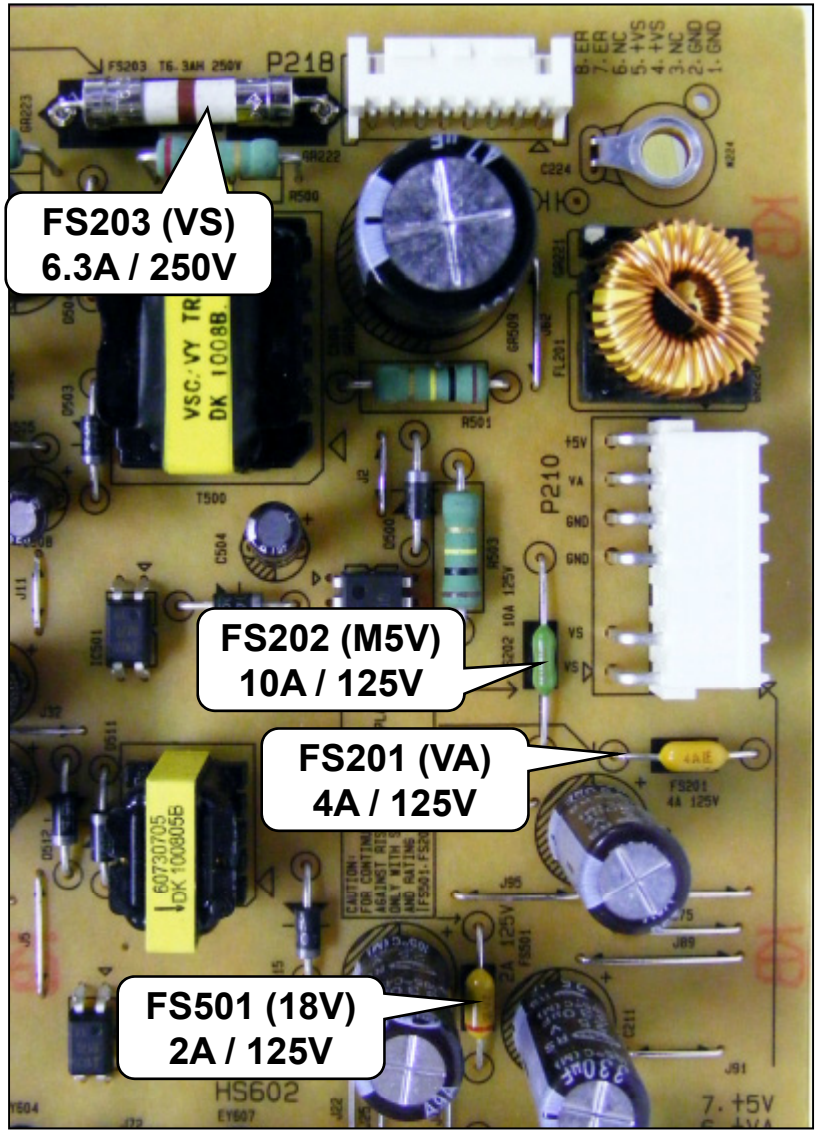
+Vy Source Test Point. Used Y-SUS Waveform development. Checked at Cathode Side D505.

Run: 190V Diode check: Open (Black lead on FGnd)
0.56V (Red lead on FGnd)

Floating Ground checks must be measured from Floating Ground. Use pins 3~12 on P214

Y-SUS Board Fuse Information





Board Disconnected Diode Check readings

FS203 VS or
FS201 Va
Open Red Lead on FG
Open Blk Lead on FG

(FS202) M5V
0.54V Red Lead on FG
1.4V Blk Lead on FG

(FS501) 18V
0.62V Red Lead on FG
1.32V Blk Lead on FG

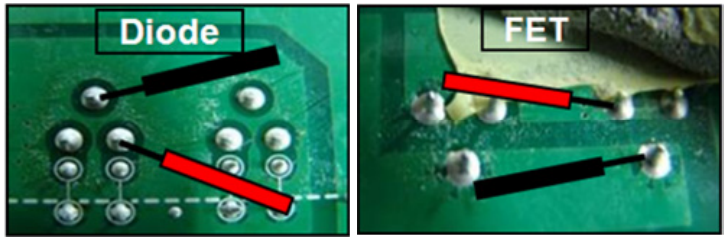
Board Connected Diode Check readings

FS201 Va or
FS203 Vs
Open

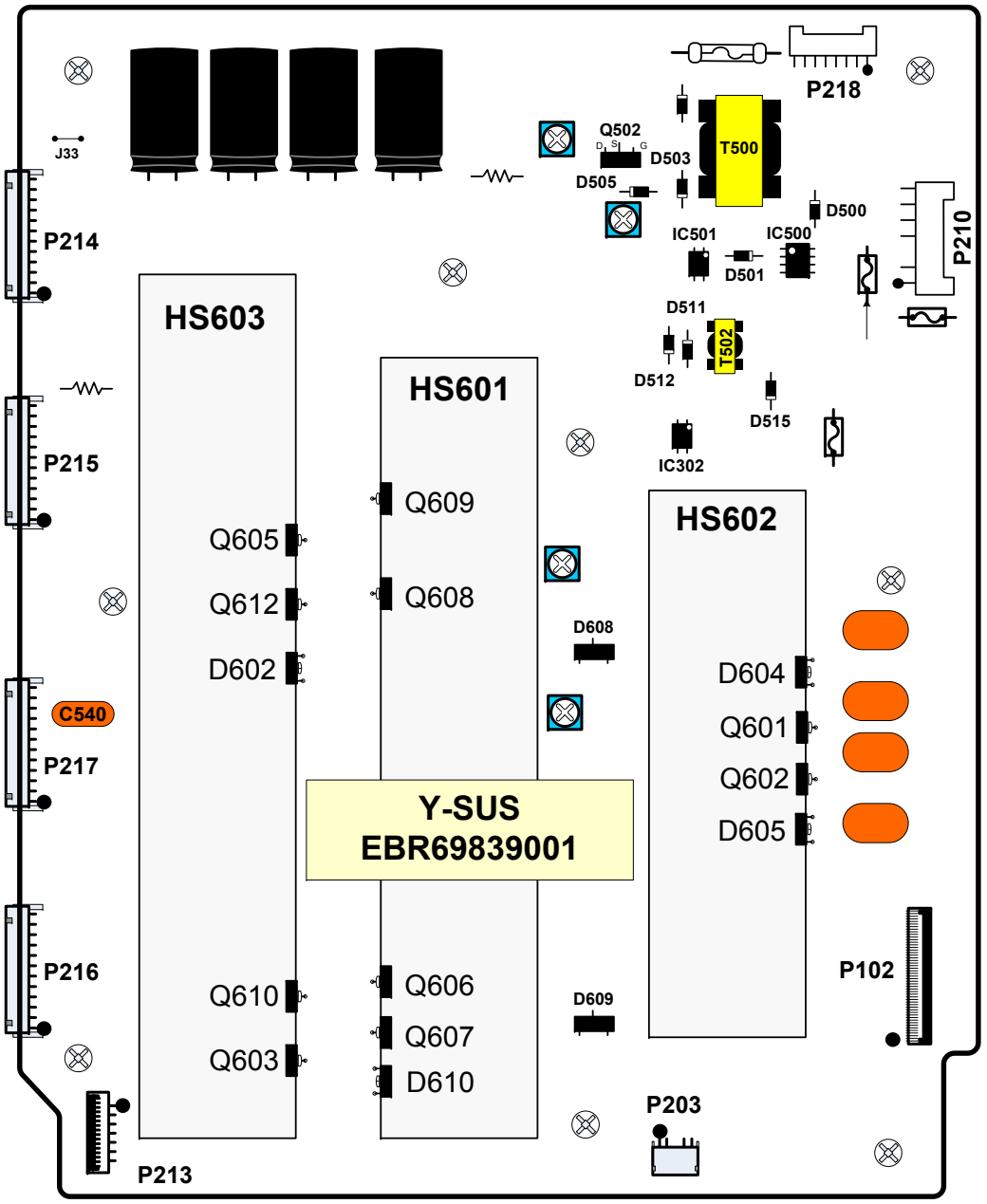
FS202 M5V
0.73V

FS501 18V
1.28V

Y-SUS FET Identification and Location

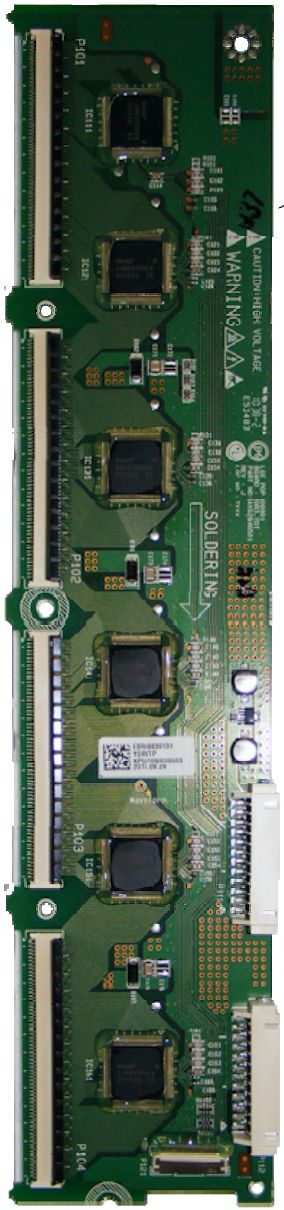


Position	Direction	Circuit No.		
HS601		D610	Q606,Q607	Q608,Q609
	Forward	0.35V ~ 0.45V	0.45V ~ 0.55V	0.45V ~ 0.55V
	Reverse	O.L. (Overload)		
HS602		D604,D605	Q601,Q602	
	Forward	0.35V ~ 0.45V	0.45V ~ 0.55V	
	Reverse	O.L. (Overload)		
HS603		D602	Q603,Q605	Q610,Q612
	Forward	0.35V ~ 0.45V	0.35V ~ 0.45V	0.4V ~ 0.5V
	Reverse	O.L. (Overload)		



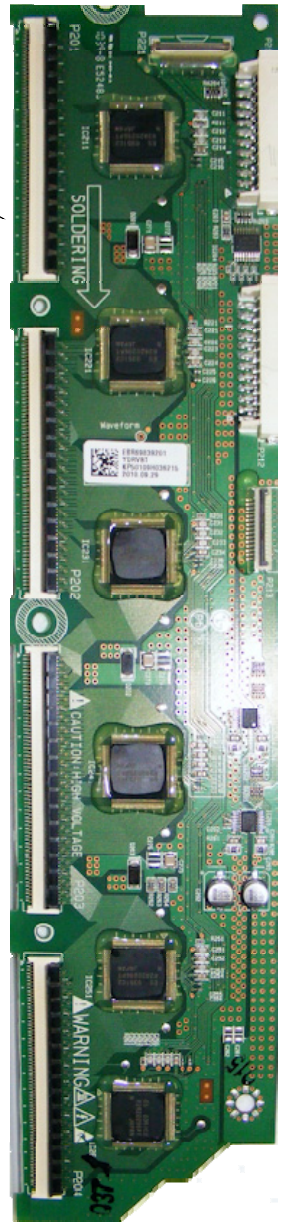
Y-DRIVE BOARD SECTION

Y-Drive Explained



Y-DRIVE UPPER (TOP)

Y-DRIVE LOWER (BOTTOM)



Y-Drive Boards work as a path supplying the Sustain and Reset waveforms which are made in the Y-Sustain board and sent to the Panel through Scan Driver IC's.

The Y-Drive Boards receive a waveform (Y-Drive) developed on the Y-SUS board then selects the horizontal electrodes sequentially starting at the top and scanning down the panel.
Scanning is synchronized by receiving Logic scan signals from the Control board.

The 50PV450 uses 12 Driver ICs on 2 Y-Drive Boards commonly called "Y-Drive Buffers" but are actually Gate Arrays connected to 1080 horizontal electrodes across the panel.

This model also does something new, Monitor 5V is sent to the Lower Y-Drive where the low voltage Data Buffer are located.

Also, The upper Y-Drive receives FG10.9V and regulates it down to FG5V for the upper and routed down to the lower Y-Drive buffers.

Y-Drive Upper Layout

p/n: EBR69839101

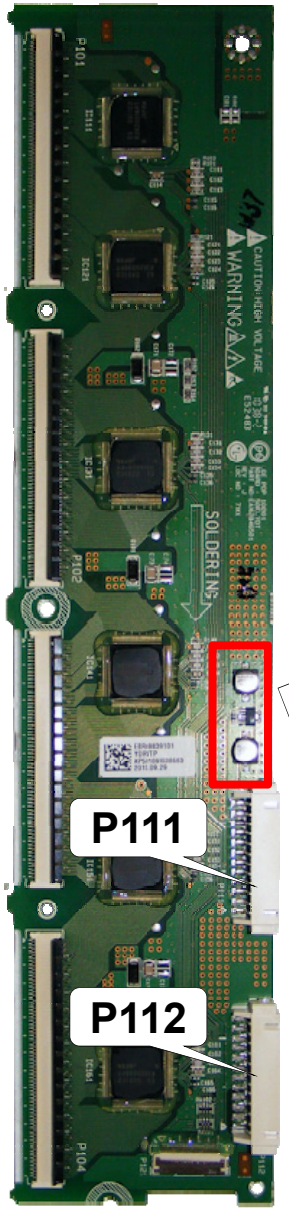
The upper Y-Drive is responsible for driving the upper half of the panel's horizontal electrodes with Y-Scan signals through the Panel's Flexible printed circuits. (540 horizontal electrodes).

The Upper Y-Drive is also responsible for developing the FG5V operational voltage for both Drive boards. It receives FG10.9V from the Y-SUS on P111 pins 11~12 and routs this voltage to IC191 which regulates it down to 5VFG.

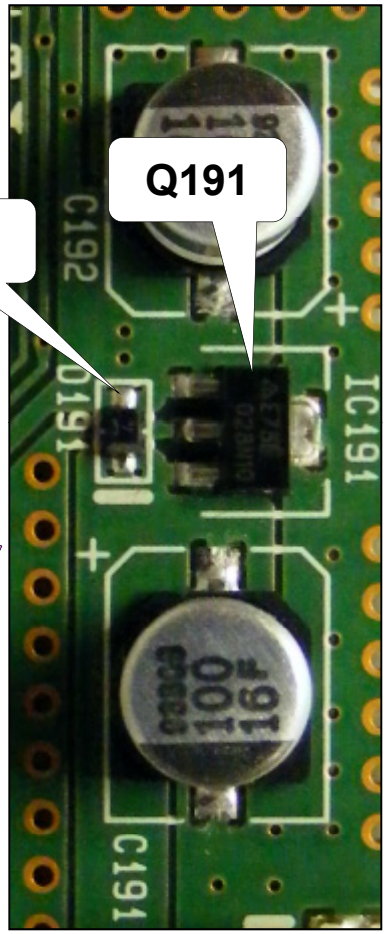
The Upper Y-Drive then delivers the 5VFG to all the buffers for their low voltage signal processing circuits. The 5VFG is also sent down to the lower Y-Drive via P121 pins 21~30 to P221 pins 1~9 for the lower Y-Drive buffers. Can not read pins because they are covered in silicon.

Warning: Never run the Y-SUS with just P121 disconnected. You must remove the Upper Y-Drive board completely.

Y-Drive Upper Floating Ground 5V Regulator (5VFG)



Floating Ground checks must be measured from Floating Ground.
Use pins 3~12 on P214



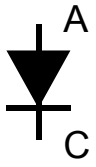
IC191

(1) 5VFG
(2) FGnd
(3) 10.9VFG

Pin	Diode Check	
1	0.42V	Red Lead on FGnd
1	2.19V	Blk Lead on FGnd
3	0.63V	Red Lead on FGnd
3	2.79V	Blk Lead on FGnd

The Upper Y-Drive is also responsible for developing the FG5V operational voltage for both Drive boards. It receives FG10.9V from the Y-SUS on P111 pins 11~12 and routs this voltage to IC191 which regulates it down to 5VFG.

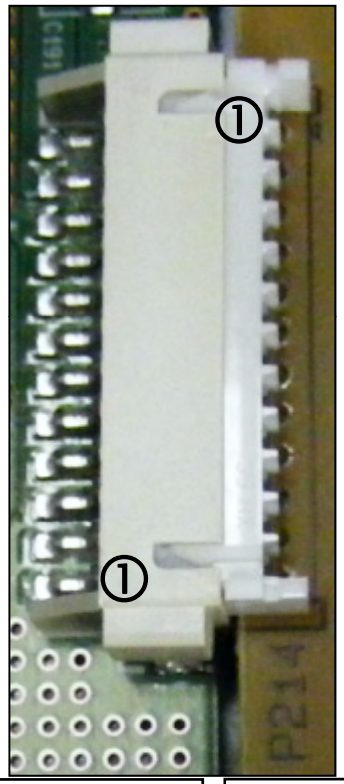
D191
Anode 5VFGnd
Cathode 10.9VFGnd



P111 Upper Y-Drive to Y-SUS Board P214 Voltage and Diode Test

Location: Top Right hand connector

P111 **P214**



Y-Drive Upper **Y-SUS Board**

Upper Y-Drive P111 to Y-SUS Board P214

Pin	Label	Run	Diode Check	Diode Check
11-12	FG10.9V	4.89V	Open	0.5V
1-10	FGnd	FGnd	FGnd	FGnd
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

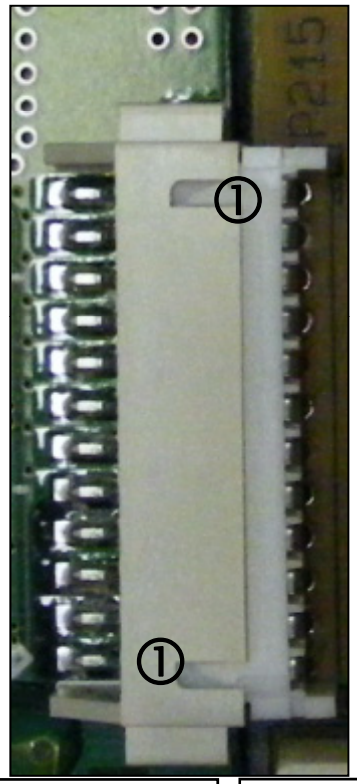
All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P112 Upper Y-Drive to Y-SUS Board P215 Voltage and Diode Test

Location: Bottom Left of board

P112 **P215**



Y-Drive Upper **Y-SUS Board**

Upper Y-Drive P112 to Y-SUS Board P215

Pin	Label	Run	Diode Check	Diode Check
6-12	FGnd	FGnd	FGnd	FGnd
5	n/c	n/c	n/c	n/c
1-4	Vscan	107V	Open	1.54V
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

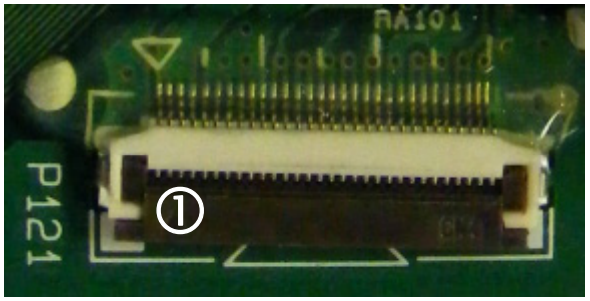
P121 Upper Y-Drive to Lower Y-Drive P221 Voltage and Diode Test

Location: Bottom of board

P121 "Upper Y-Drive" to P221 "Lower Y-Drive"

Pin	Label	Run	
1~4	SUS_DN (FG)	FG	Can not read the pins because they are covered in silicon
11	YSUS_DATA	0V	
12	YT_OCR	2.4V	
13	YT_OC1	2.2V	
14	YT_LE(STB)	2.6V	
15	YT_CLK	0.8V	
16	YT_DATA	0V	
17~20	SUS_DN (FG)	FG	
21~23	FG5V	4.97V	
27~30	FG5V	FG	

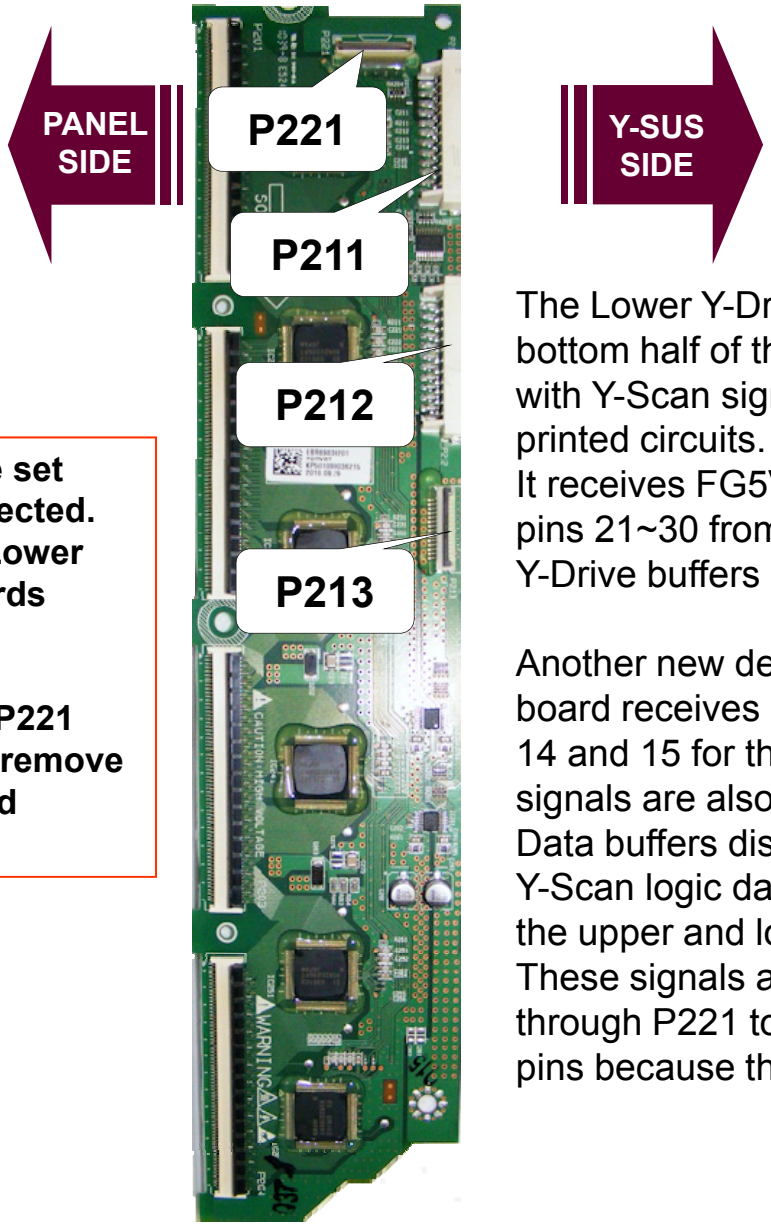
P121



All voltages are from Floating Ground

Y-Drive Lower Layout

p/n: EBR69839201



Warning: Never run the set with just P213 disconnected. You must remove the Lower and Upper Y-Drive boards completely.

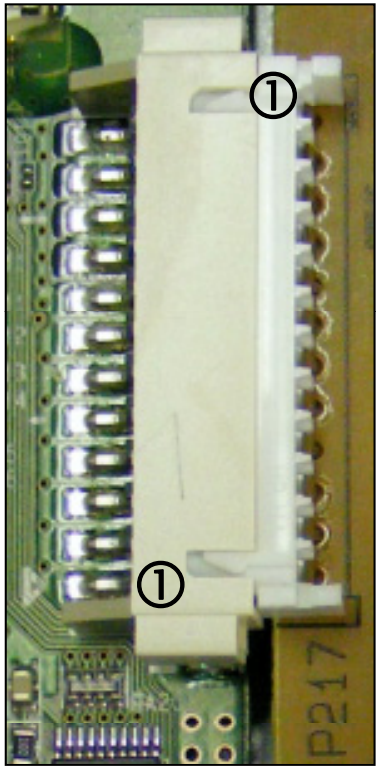
Never run the set with P221 unplugged unless you remove the Upper Y-Drive board completely.

The Lower Y-Drive is responsible for driving the bottom half of the panel's 540 horizontal electrodes with Y-Scan signals through the Panel's Flexible printed circuits.
It receives FG5V from the Upper Y-Drive on P221 pins 21~30 from P121 pins 1~9 for the lower Y-Drive buffers low voltage signal processing.

Another new development is that the lower Y-Drive board receives Chassis Ground and M5V P213 pins 14 and 15 for the Data buffers. The Y-Scan logic signals are also related to chassis ground and the Data buffers distribute the
Y-Scan logic data to all the Buffers, (Gate arrays) on the upper and lower Y-Drive boards.
These signals are routed to the Upper Y-Drive through P221 to P121 on the upper. Can not read pins because they are covered in silicon.

P211 Lower Y-Drive to Y-SUS Board P217 Voltage and Diode Test

Location: Bottom Left of board



Y-Drive Upper | **Y-SUS Board**

P211 "Lower Y-Drive" to "Y-SUS" P217

Pin	Label	Run	Diode Check	Diode Check
9-12	Vscan	107V	Open	1.54V
8	n/c	n/c	n/c	n/c
1-7	FGnd	FGnd	FGnd	FGnd
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

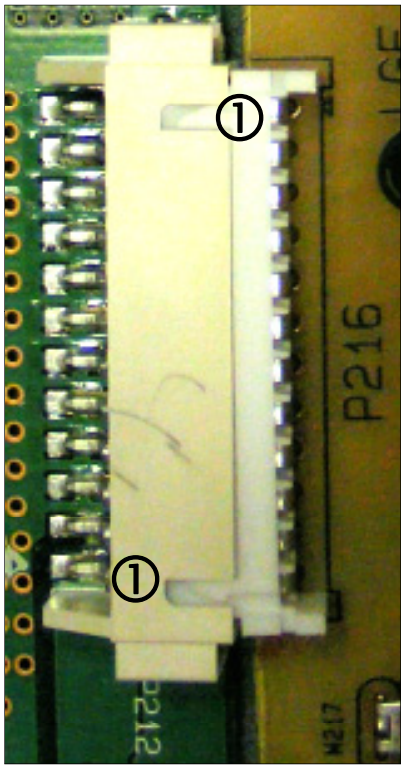
All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P212 Lower Y-Drive to Y-SUS Board P216 Voltage and Diode Test

Location: Bottom Left of board

P212 **P216**



Y-Drive Upper **Y-SUS Board**

Y-Drive P212 to Y-SUS Board P216

Pin	Label	Run	Diode Check	Diode Check
3-12	FGnd	FGnd	FGnd	FGnd
1-2	Vscan	107V	Open	1.54V
		Black Lead on Floating Gnd		Red Lead on Floating Gnd

All readings from Floating Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P221 Lower Y-Drive to Upper Y-Drive P121 Voltage and Diode Test

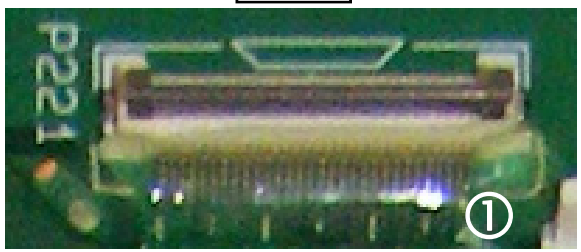
Location: Top of board

P221 "Lower Y-Drive" to P121 "Upper Y-Drive"

Pin	Label	Run
1~4	FG5V	5V
5-9	FGnd	0V
12	YT_OCR	2.4V
13	YT_OC1	2.2V
14	YT_LE(STB)	2.6V
15	YT_CLK	0.8V
16	YT_DATA	0V
17~20	SUS_DN (FG)	FG
21~23	FG5V	4.97V
24~30	SUS_DN (FG)	FG

Can not read the pins because they are covered in silicon

P221



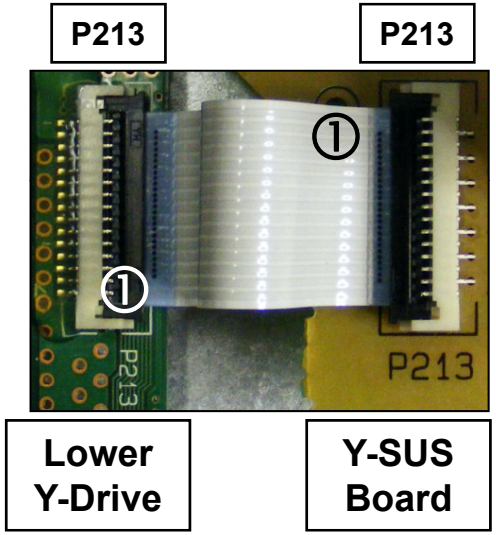
All voltages are from Floating Ground

P213 Lower Y-Drive to Y-SUS Board P213 Connector (Logic Signals)

TIP: This connector does not come with a new Y-SUS or Y-Drive.

TIP: Use C540 Left leg to check the Y-Scan signal if the Y-Drive boards are removed

Note: The Lower Y-Drive board receives Monitor 5V from the Y-SUS.



P212 "Y-SUS" to "Lower "Y-Drive" P213

Pin	Label	Run	Diode Check	Diode Check
15	M5V	4.89V	1.9V	0.55V
14	M5V	4.89V	1.9V	0.55V
13	OC2_B	2.63V	2.08V	0.63V
12	Gnd	Gnd	Gnd	Gnd
11	DATA_B	0V	2.08V	0.63V
10	Gnd	Gnd	Gnd	Gnd
9	OC1_B	2.2V	Open	0.63V
8	OC2_T	2.2V	2.08V	0.63V
7	Gnd	Gnd	Gnd	Gnd
6	DATA_T	2.8V	2.08V	0.63V
5	Gnd	Gnd	Gnd	Gnd
4	OC1_T	0.86V	2.34V	0.63V
3	Gnd	Gnd	Gnd	Gnd
2	CLK	FG	2.08V	0.63V
1	STB	4.9V	2.08V	0.63V
			Red Lead on pin	Black Lead on pin

Black Lead on Chassis Gnd

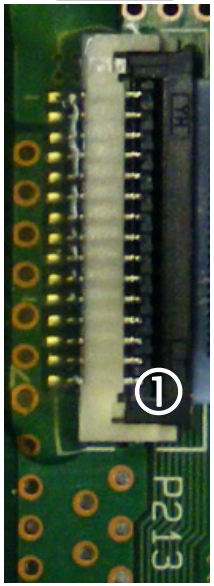
All voltage readings taken from Chassis Ground

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

Lower Y-Drive Board P213 Connector Waveforms

Note: The Lower Y-Drive board receives Monitor 5V from the Y-SUS.

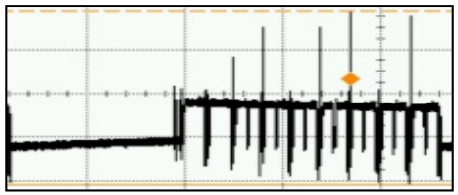
P213



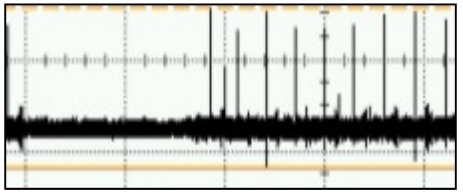
P213 Y-SUS to Lower Y-Drive P213

Pin	Label
Pin	Label
15	M5V
14	M5V
13	OC2_B
12	Gnd
11	DATA_B
10	Gnd
9	OC1_B
8	OC2_T
7	Gnd
6	DATA_T
5	Gnd
4	OC1_T
3	Gnd
2	CLK
1	STB

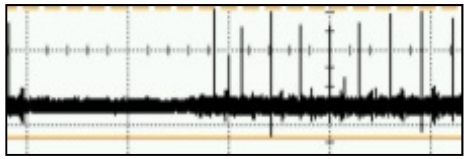
Pin 13 (19.9V p/p)



Pin 6 (8.47V p/p)

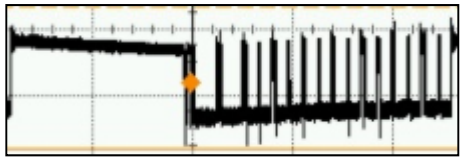


Pin 11 (8.62V p/p)

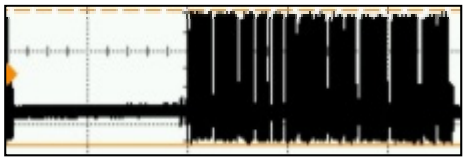


Pin 4 (9V p/p)

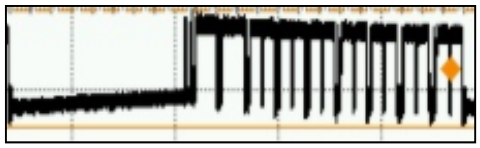
Pin 9 (10.67V p/p)



Pin 2 (9.08V p/p)



Pin 8 (10.67V p/p)



Pin 1 (11.15V p/p)

All scope settings at 5mSec per/div / 5V per/div
All signals taken from Chassis Ground

Removing (Panel) Flexible Ribbon Cables from Y-Drive Upper or Lower

Pictures are from a different model, but the process is the same.

To remove the Ribbon Cable from the connector first carefully lift the Locking Tab from the back and tilt it forward (lift from under the tab as shown in Fig 1).
The locking tab must be standing straight up as shown in Fig 2.
Lift up the entire Ribbon Cable gently to release the Tabs on each end. (See Fig 3)
Gently slide the Ribbon Cable free from the connector.

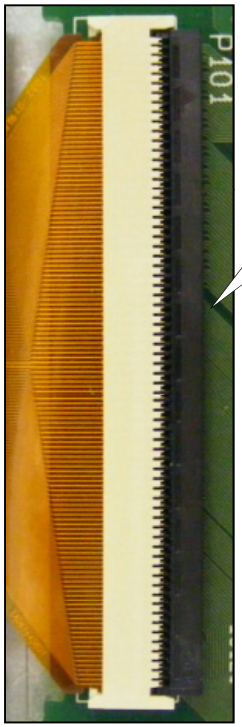


Fig 1

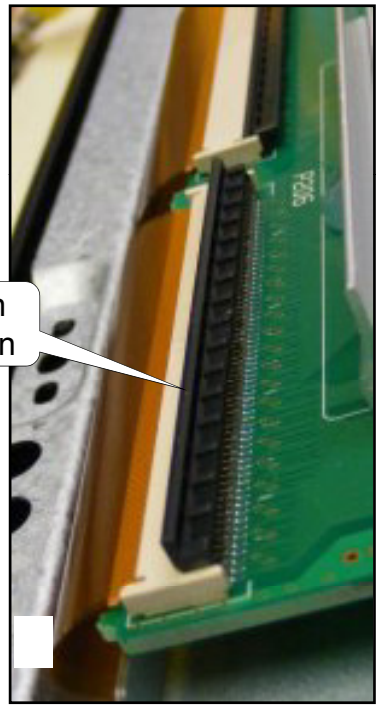


Fig 2

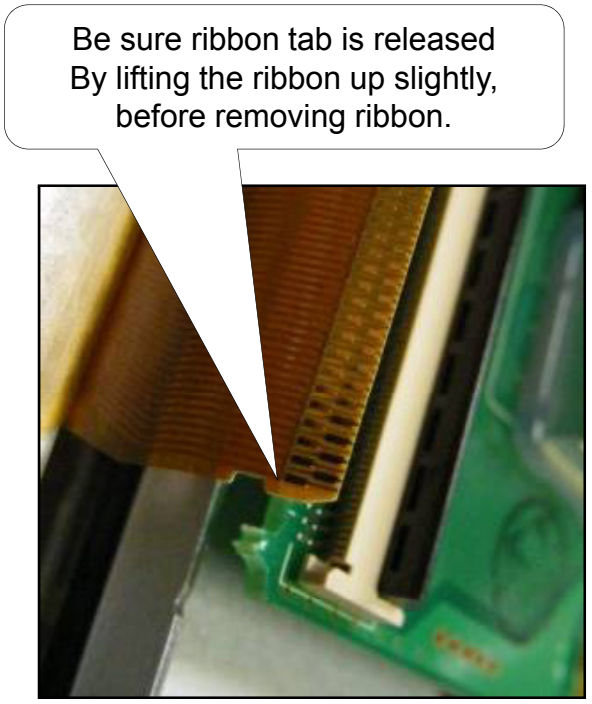


Fig 3

To reinstall the Ribbon Cable, carefully slide it back into the slot see (Fig 3), be sure the Tab is seated securely and press the Locking Tab back to the locked position see (Fig 2 then Fig 1).

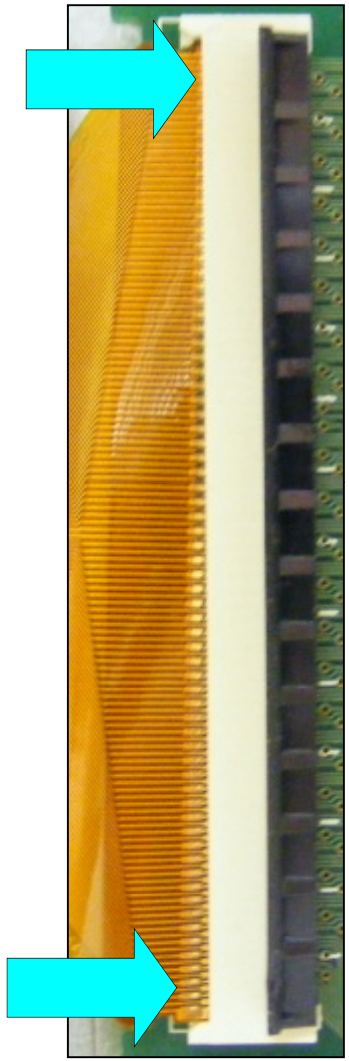
Incorrectly Seated Y-Drive Flexible Ribbon Cables

The Ribbon Cable is clearly improperly seated into the connector. You can tell by observing the line of the connector compared to the FPC, they should be parallel.

The Locking Tab will offer a greater resistance to closing in the case.

Note the cable is crooked in this case because the Tab on the Ribbon cable was improperly seated at the top. This can cause bars, lines, intermittent line and other abnormalities in the picture.

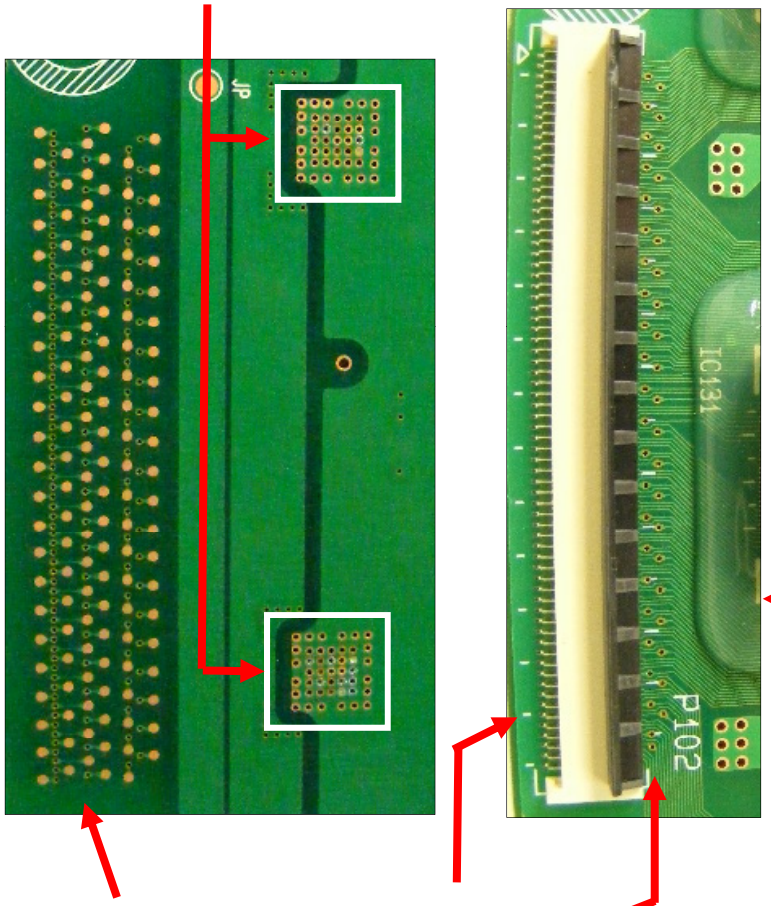
Remove the ribbon cable and re-seat it correctly.



HOW TO CHECK FOR A SHORTED BUFFER IC

BACK SIDE **FRONT SIDE**

BUFFER IC FLOATING GROUND (FGnd)



FRONT SIDE OF Y-DRIVE BOARD

Any of these output lugs can be tested.

Look for shorts indicating a defective Buffer IC

Using the "Diode Test" on the DVM, check the pins for shorts or abnormal loads.

RED LEAD On Floating Ground

Indicated by white outline

BLACK LEAD On "ANY" Output Lug Reads 0.78V

Reversing the leads reads Open

8 Ribbon cables communicating with the Panel's (Horizontal Electrodes) totaling 1080 lines determining the Panel's Vertical resolution pixel count.

Z-SUS SECTION

This Section of the Presentation will cover troubleshooting the Z-SUS Board Assembly.
Upon completion of this section the Technician will have a better understanding of the circuit and be able to locate test points needed for troubleshooting and all alignments.

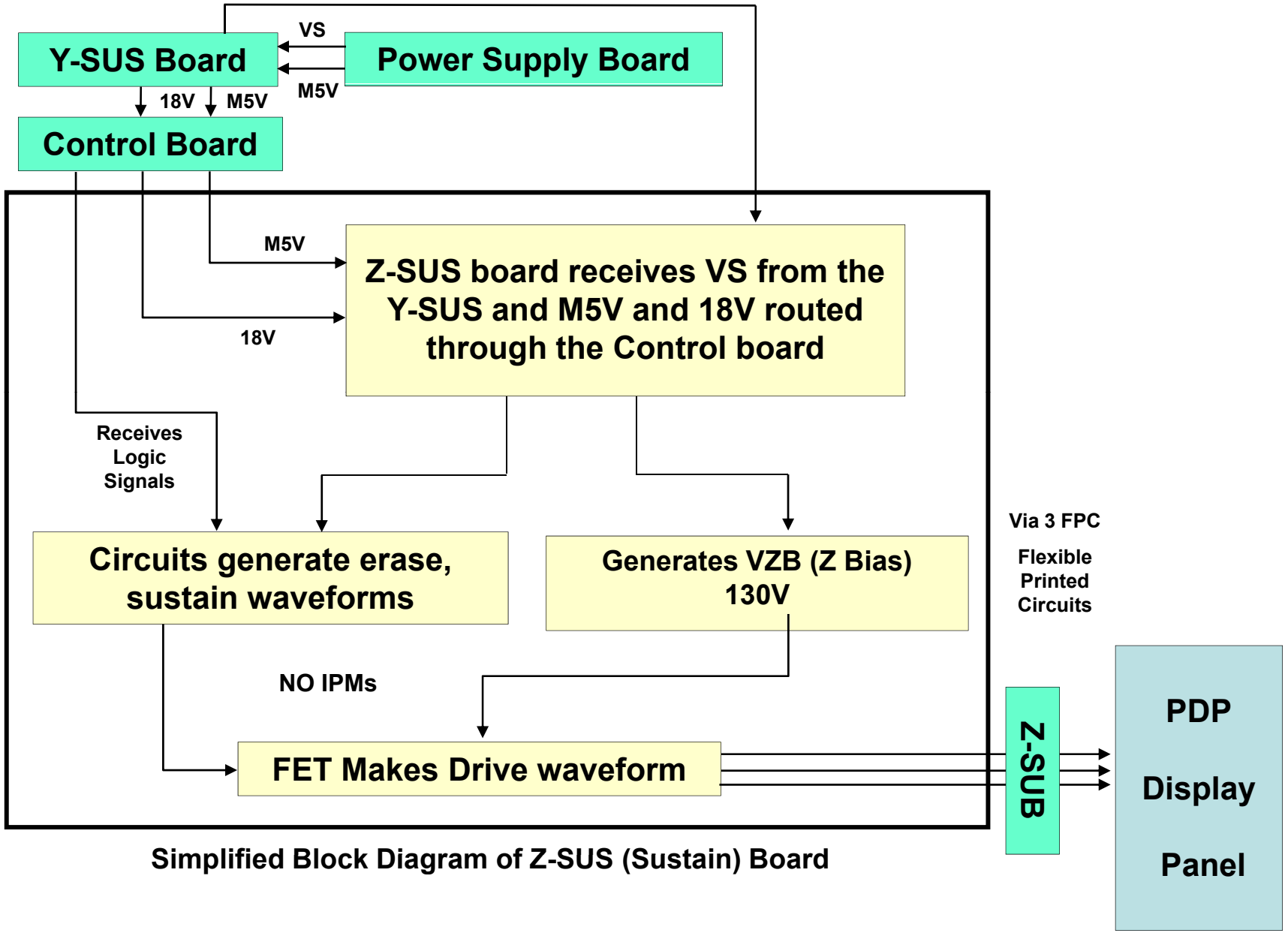
Locations

- DC Voltage and Waveform Test Points
- Z BIAS Alignment
- Diode Mode Test Points

Operating Voltages

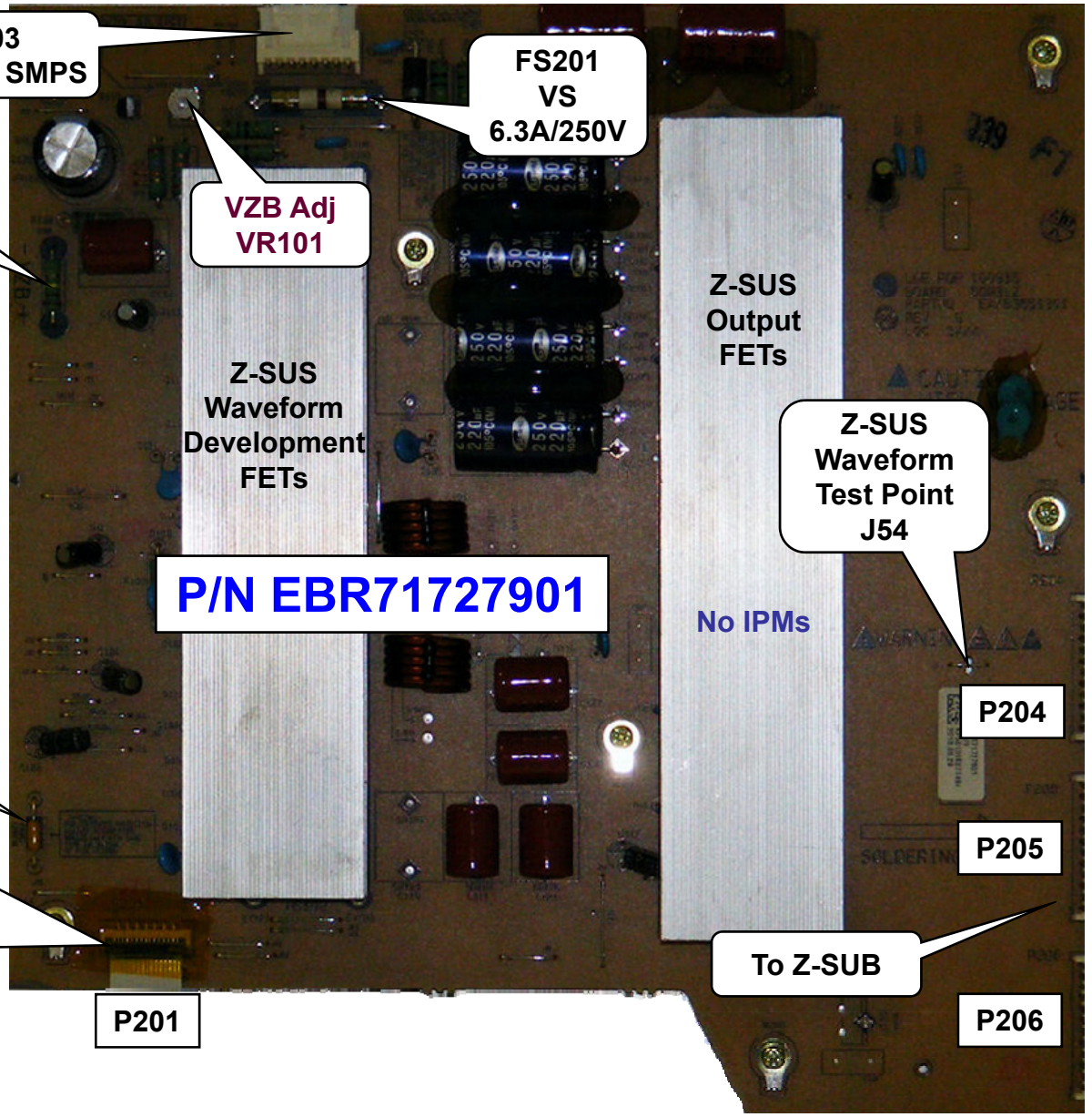
Power Supply Supplied	VS	
	M5V	Routed through the Y-SUS then to the Control Board then to the Z-SUS
Y-SUS Supplied	18V	Generated on the Y-SUS then to the Control Board then to the Z-SUS. Control board does not use the 18V.
Developed on Z-SUS	Z Bias	

Z-SUS Block Diagram



Simplified Block Diagram of Z-SUS (Sustain) Board

Z-SUS Board Component Identification



50PV450 Z-SUS Board Drawing

P203
7-8) Gnd
6) n/c
4-5) VS
3) n/c
1-2) ER

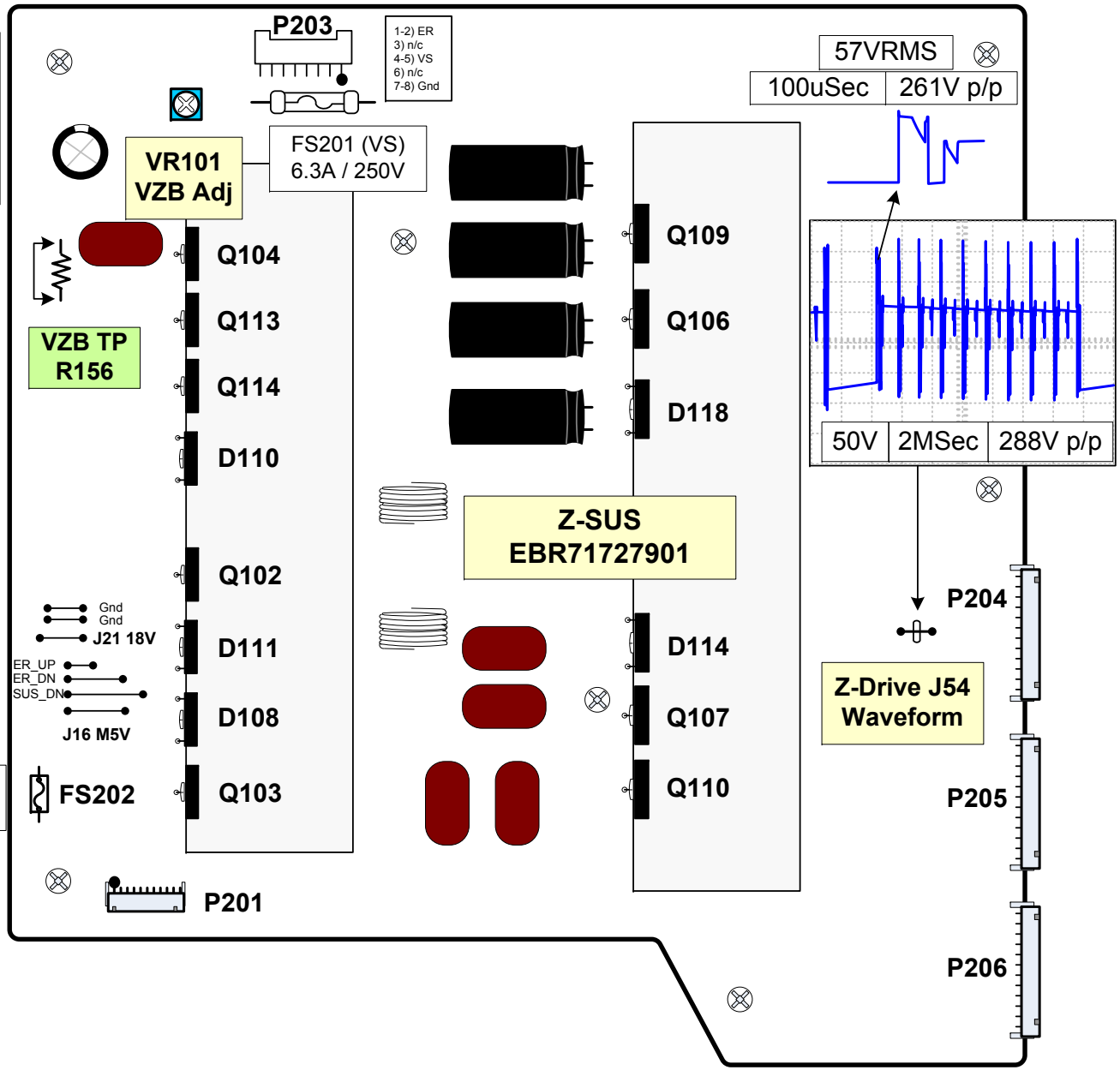
Example:

Model : PDP 50R3###
Voltage Setting: 5V/ Va:55/ Vs:201
N.A. / -190 / 150 / N.A. / 130
Max Watt : 360 W (Full White)

VZB (Z Bias)

To run the Z-SUS stand-alone:
Jump VS from SMPS to pins 4 or 5 of P203. Jump +5V from SMPS to fuse FS202. Jump 17V from SMPS to J21. Leave Connector P201 connected to Control Board.
J54 290V p/p (More square shape).

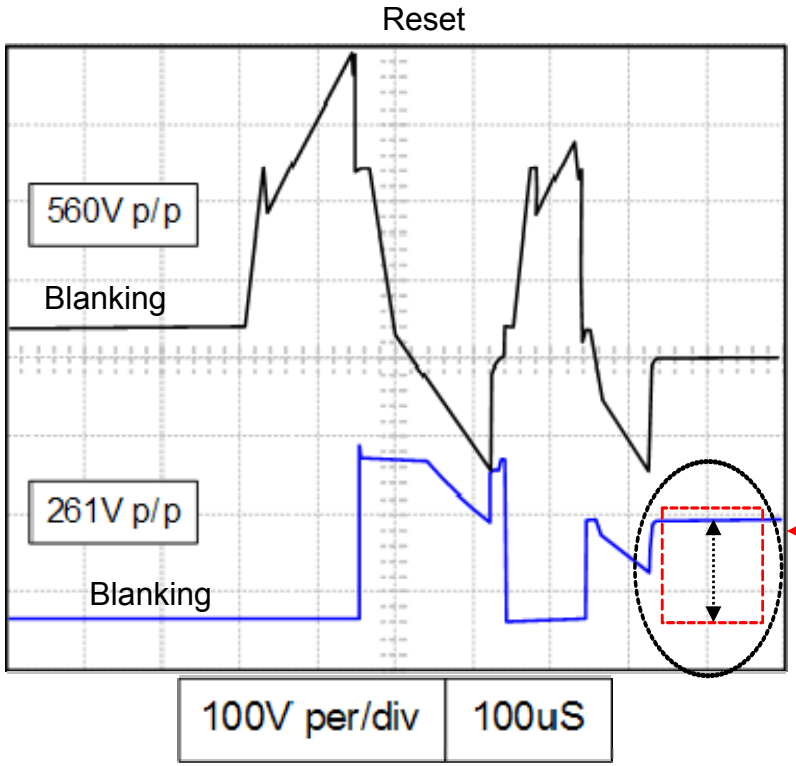
P201	
1-2) 18V	18.34V
3) n/c	(n/c)
4-5) M5V	4.89V
6-7) Gnd	Gnd
8) SUS_DN	0.73V
9) CTRL_EN	0.06V
10) SUS_UP	0.15V
11) VZB2	2.49V
12) ER_DN	0.1V
13) VZB1	2.53V
14) ER_UP	0.11V
15) ZBIAS	1.89V



Z-SUS Waveform

The Z-SUS (in combination with the Y-SUS) generates a SUSTAIN Signal and an ERASE PULSE for generating SUSTAIN and DISCHARGE in the Panel.

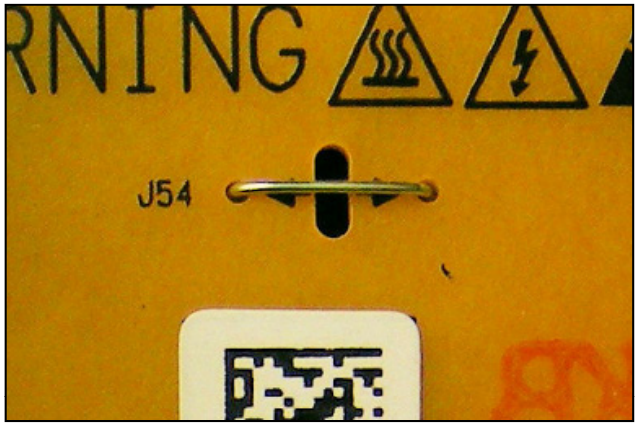
This waveform is supplied to the panel through Z-SUB and then to FPC (Flexible Printed Circuit) connections P201, P202 and P203.



Y Drive Waveform

Z Drive Waveform

Location: Center Right of Z-SUS board



Oscilloscope Connection Point.

J54 to check Z Output waveform.

Right Hand Side Center.

VZB VR101 manipulates the offset of the Z-Drive waveform segment.

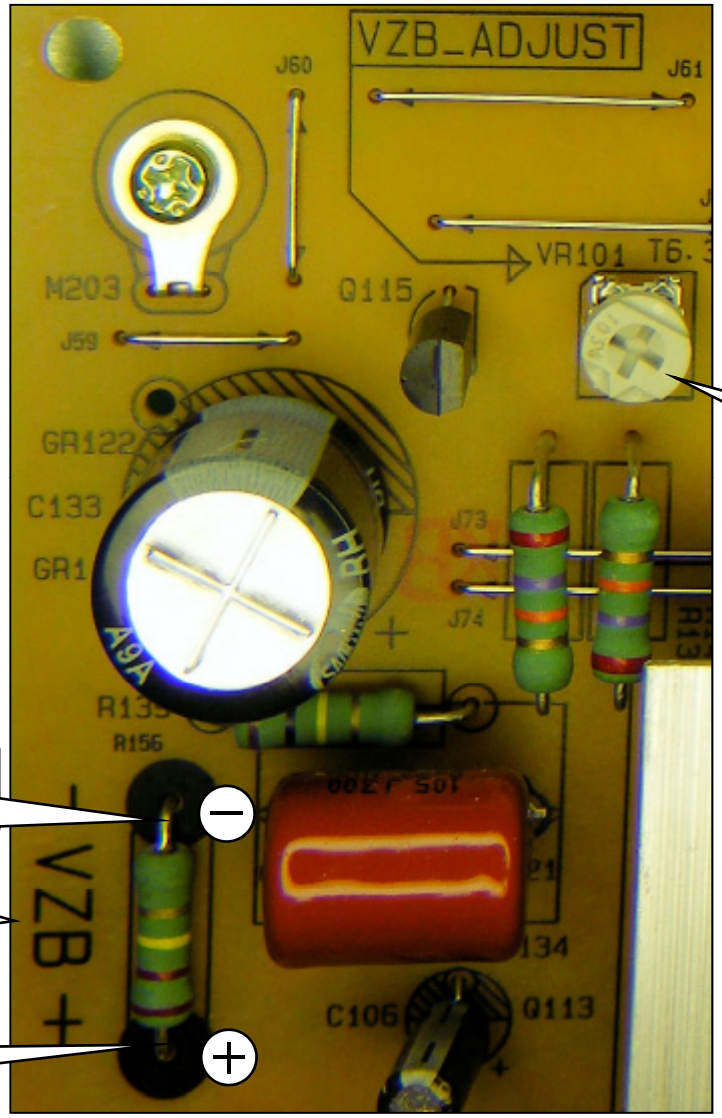
VZB (Z-Bias) voltage 130V ± 1/2V

TIP: The Z-Bias (VZB) Adjustment is a DC level adjustment. This is only to show the effects of Z-Bias on the waveform.

This Waveform is just for reference to observe the effects of Z Bias adjustment

Z-Bias (VZB) VR101 Adjustment

Location Top Left of Z-SUS Board



Negative Lead

VZB (Z Bias) R156

Positive Lead

Example of a voltage label:

Model : PDP 50R3###
Voltage Setting: 5V/ Va:55/ Vs:201
N.A. / -190 / 150 / N.A. / 130
Max Watt : 360 W (Full White)

VZB (Z-Bias)

Read the Voltage Label on the back top center of the panel when adjusting VR101.

VZB (Z-Bias) Adjust VR101

Set should run for 10 minutes, this is the "Heat Run" mode. Set screen to "White Wash" mode or 100 IRE White input.

Adjust VR101 VZ (Z-Bias) while reading across R156 to match your Panel's Voltage Label (± 1/2V)

P203 Z-SUS Connector to Y-SUS P218 Voltages and Diode Checks

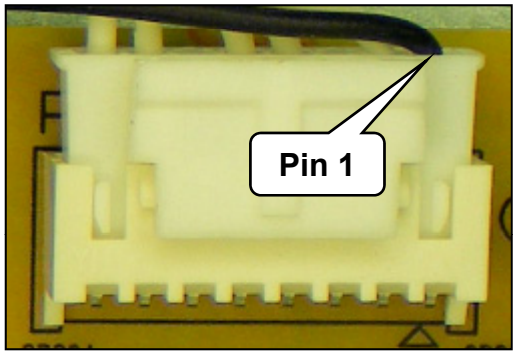
Voltage and Diode Mode Measurements

P203 "Z-SUS“ to "Y-SUS" P218

Pin	Label	Run	Diode Check
1~2	ER_PASS	*98V~102V	Open
3	n/c	n/c	n/c
4~5	**+Vs**	***201V**	**Open**
6	n/c	n/c	n/c
7~18	Gnd	Gnd	Gnd

* Note: This voltage will vary in accordance with Panel Label

P203 Location:
Top Left of Board



There are no Stand-By voltages on this connector

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

P201 Z-SUS Connector to Control P2 Voltages and Diode Checks

Voltage and Diode Mode Measurements

P201 "Z-SUS Board" to P2 "Control"

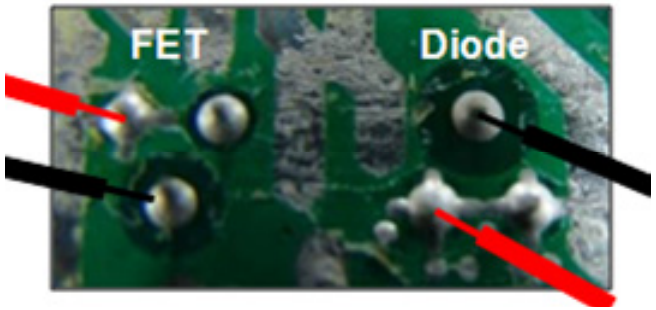
Pin	Label	Run	Diode Check
1	**+18V**	**18.34V**	**Open**
2	**+18V**	**18.34V**	**Open**
3	n/c	n/c	1.52V
4	**+5V (M5V)**	**4.89V**	**1.52V**
5	**+5V (M5V)**	**4.89V**	**1.52V**
6	Gnd	Gnd	Gnd
7	Gnd	Gnd	Gnd
8	SUS_DN	0.73V	Open
9	CTRL_EN	0.06V	Open
10	SUS_UP	0.15V	Open
11	VZB2	2.49V	Open
12	ER_DN	0.1V	Open
13	VZB1	2.53V	Open
14	ER_UP	0.87V	Open
15	ZBIAS	1.9V	Open

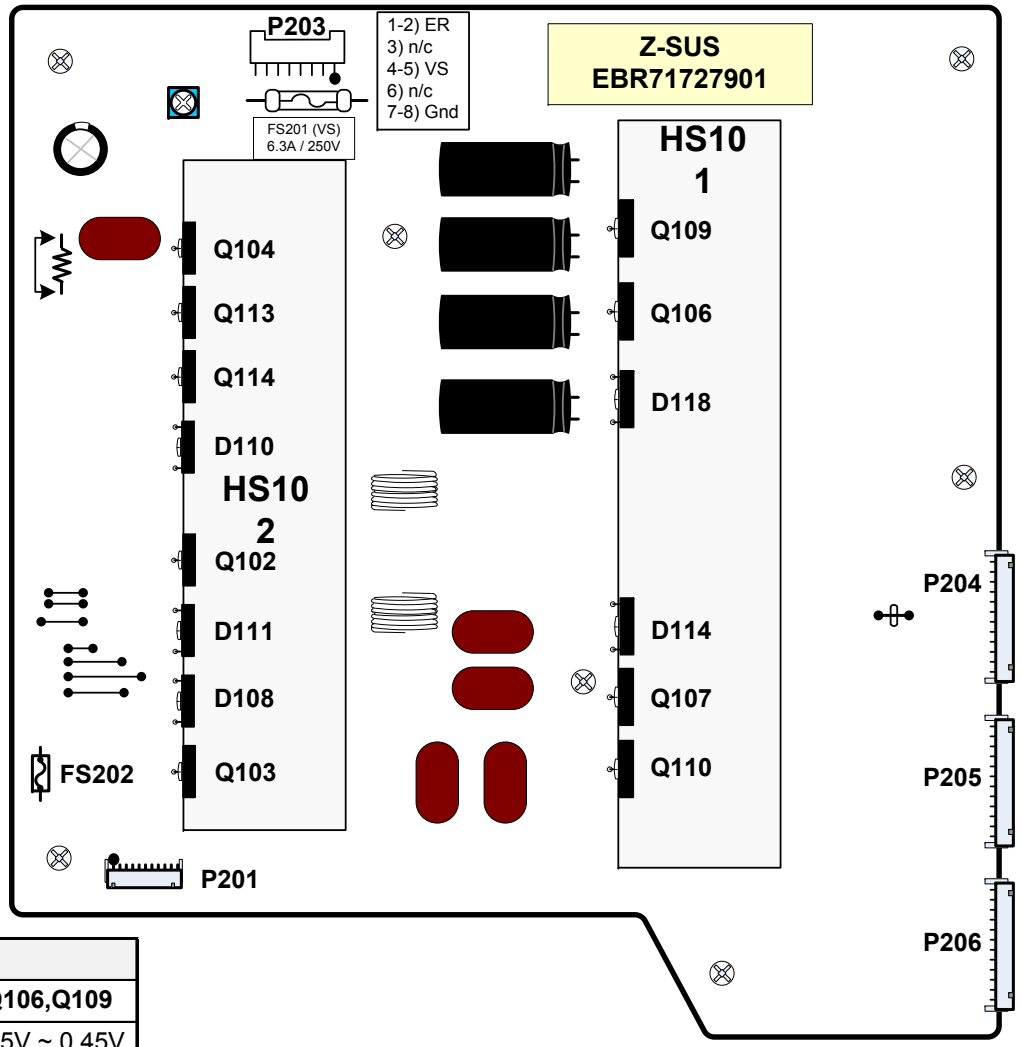
There are no Stand-By voltages on this connector

P201 Location:
Bottom Left hand side

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

50PV450 Z-SUS Board FET Locations





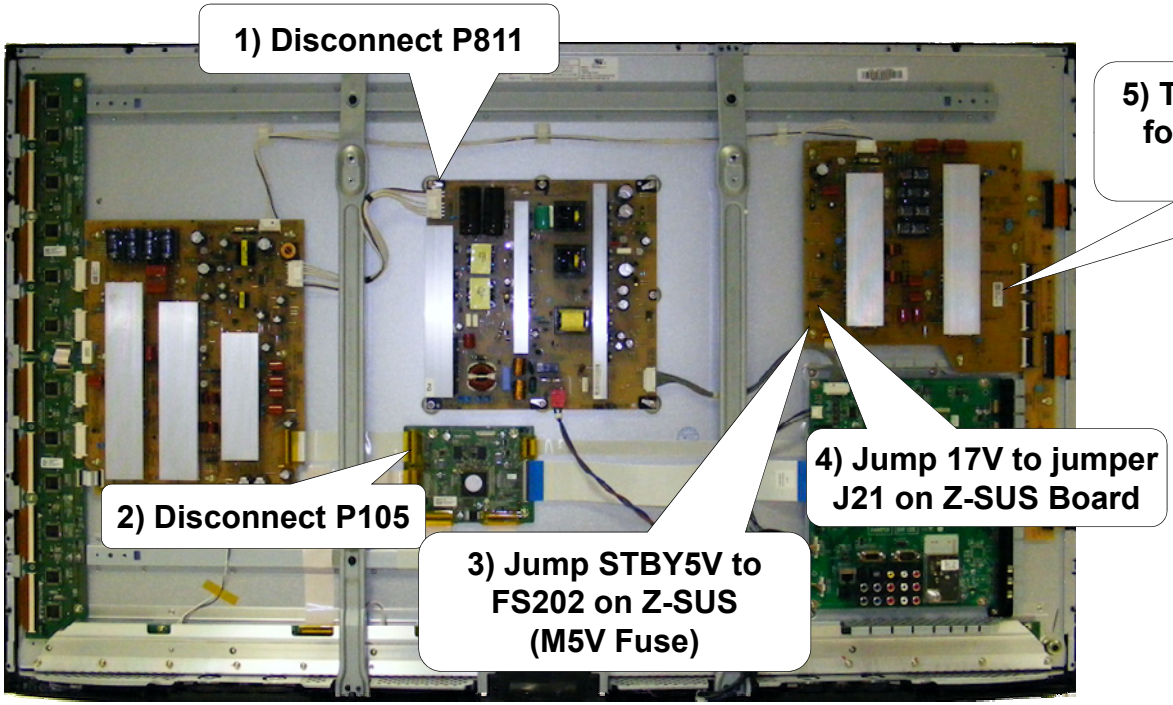
Position	Direction	Circuit No.		
		D114,D118	**Q107,Q110**	**Q106,Q109**
HS101	Forward	0.35V ~ 0.45V	0.35V ~ 0.45V	0.35V ~ 0.45V
	Reverse	O.L. (Overload)		
		D109,D110,D108,D111	**Q104,Q113,Q114**	**Q102,Q103**
HS102	Forward	0.35V ~ 0.45V	0.5V ~ 0.6V	0.4V ~ 0.55V
	Reverse	O.L. (Overload)		

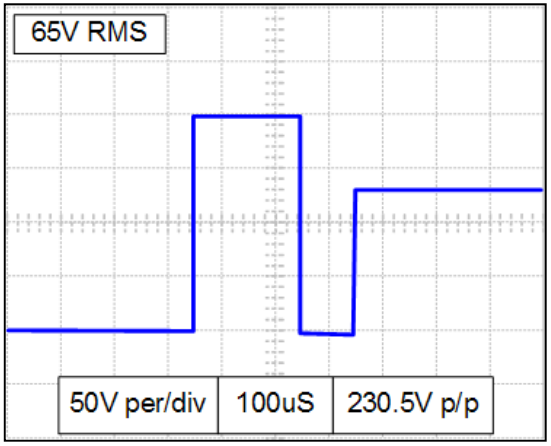
How to Check the Z-SUS Stand-Alone

The Power Supply should be producing VS or you can substitute voltage matching VS from an external source to either pin 1 or 2 P102 on the Z-SUS board.

The Power Supply should be producing M5V or you can substitute Stand-By 5V or any 5V from an external source to the 5V Fuse on the Z-SUS (FS202). Note: The 5V will be routed back to the Control Board for power through the P201 to P2 connector.

The Power Supply should be producing 17V or you can substitute voltage matching 17V from an external source to either pins 1 or 2 on connector P2 on the Control board.





Tip: If the DC to DC converter generating 18V is running on the Y-SUS, you can jump any 5V to the Y-SUS M5V input pin, leave P105 connected and there will be no need to jump the 17V or the M5V to the Z-SUS.

CONTROL BOARD SECTION

This Section of the Presentation will cover troubleshooting the Control Board Assembly. Upon completion of this section the Technician will have a better understanding of the circuit and be able to locate test points needed for troubleshooting.

- DC Voltage and Waveform Test Points
- Diode Mode Test Points

Signals

Main Board Supplied — Panel Control and LVDS (Video) Signals

Control Board Generated — Y-SUS and Z-SUS Drive Signals (Sustain)
Y-Drive Board Scan Signals (Gate Address)
X Board Drive Signals (RGB Address)

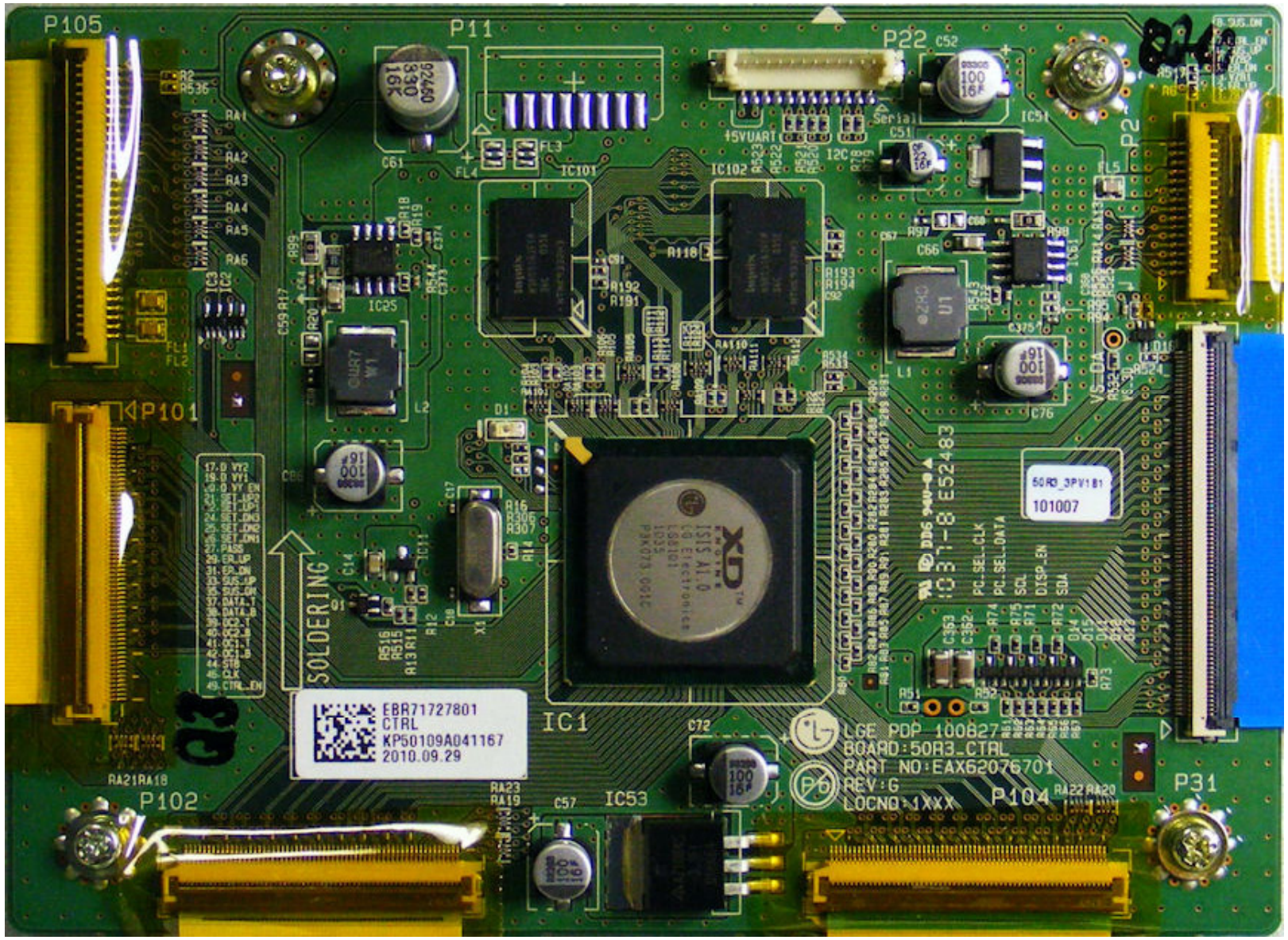
Operating Voltages

Y-SUS Supplied — +5V (M5V) Developed on the SMPS
+18V (Routed to the Z-SUS)
(Not used by the Control Board)

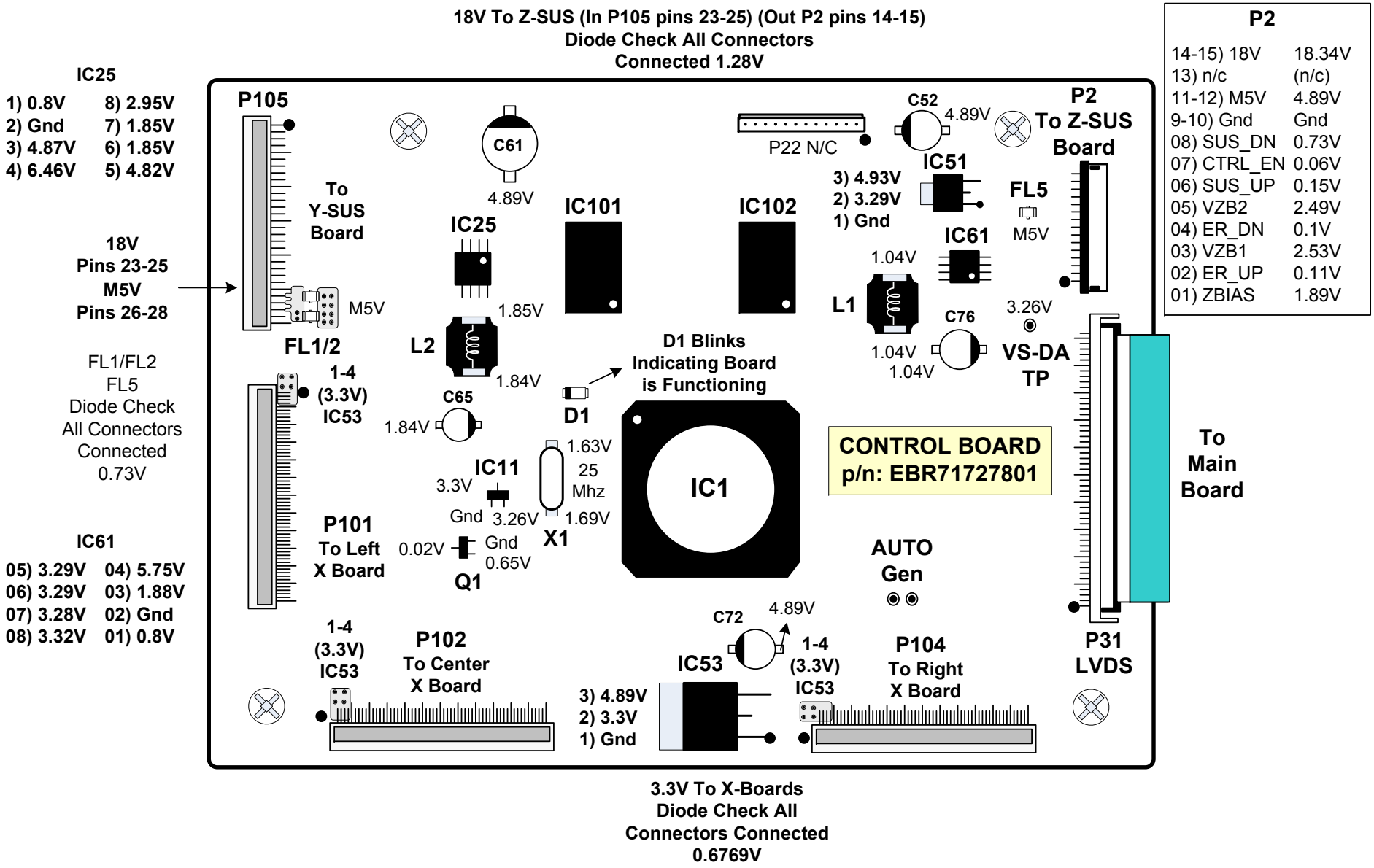
Developed on the Control Board — +1.0V (IC61) for internal use
+1.8V (IC52) for internal use. *Silk screened as IC25.*
+3.3V (IC51) for LVDS Power
+3.3V (IC53) for the X-Boards (TCPs)

Control Board Component Identification

p/n: EBR71727801



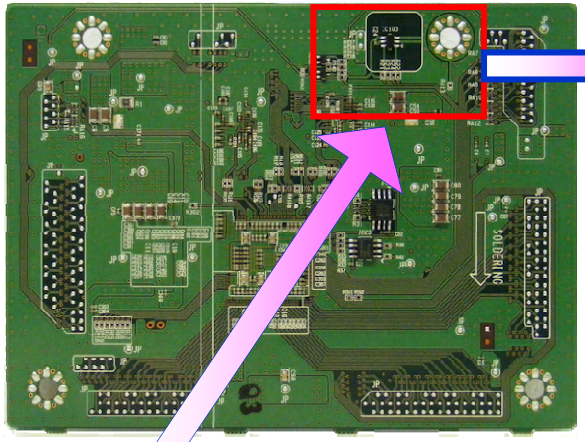
50PV450 Control Board Layout Drawing

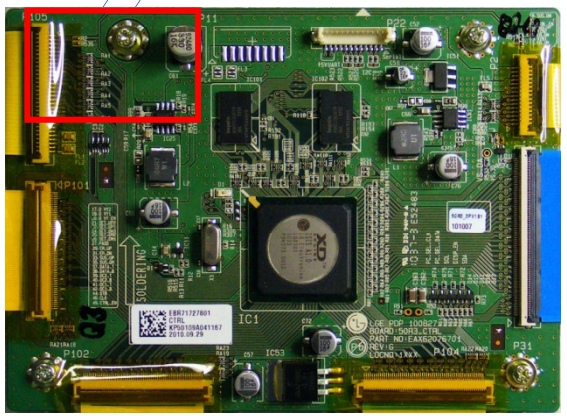


Control Board Temperature Sensor Location (Chocolate)

The panel is monitored for temperature. The panel's temperature is transferred through the (Chocolate) to the Temp. Sensor on the back of the board.

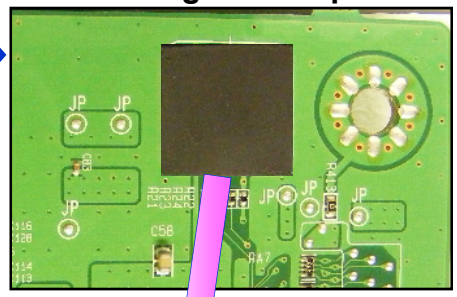
BACK SIDE OF THE BOARD

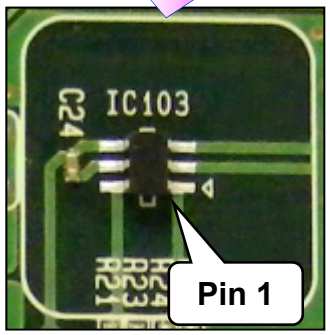




CONTROL BOARD TEMPERATURE SENSOR LOCATION

With Chocolate (Heat Transfer Material) Covering the Temp IC.

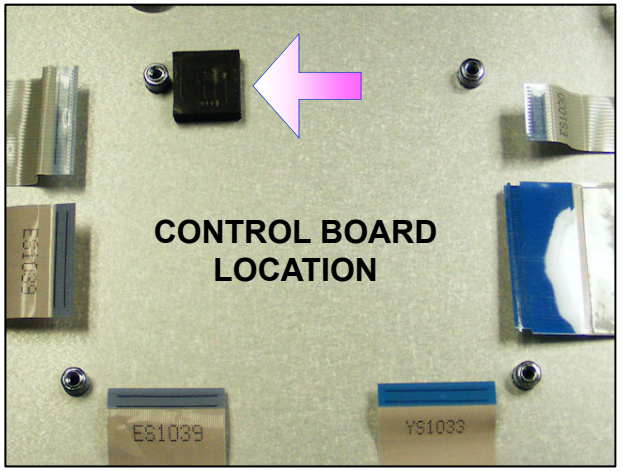




IC103

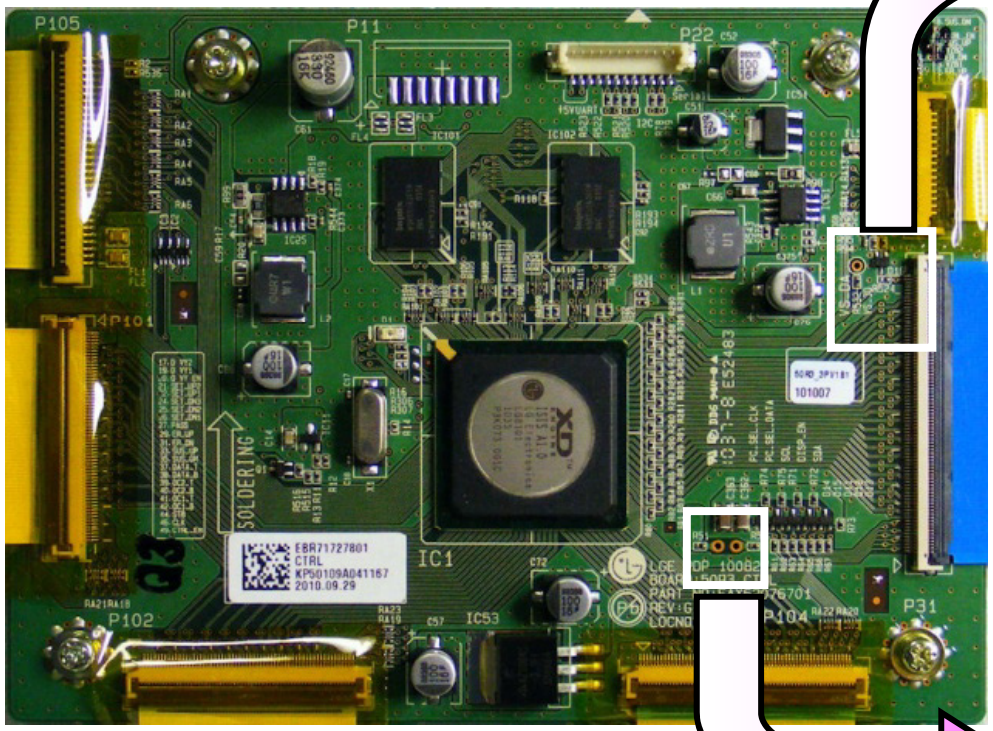
04) 3.3V	03) Gnd
05) Gnd	02) Gnd
06) 3.3V	01) 3.3V

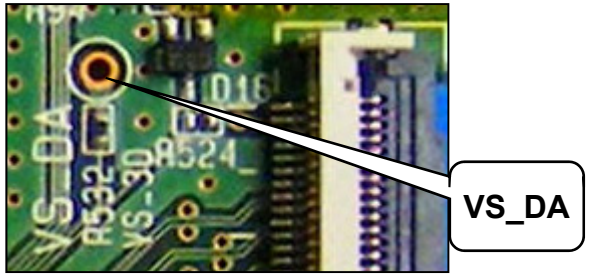
The Chocolate (Heat Transfer Material) may stick to the Panel. Be sure to put it in the right place if the board is removed.

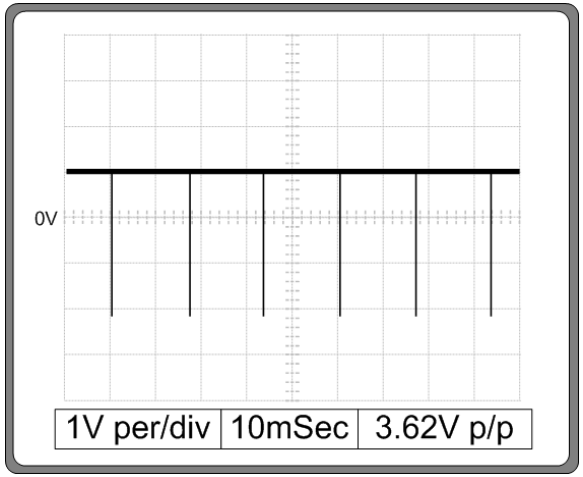


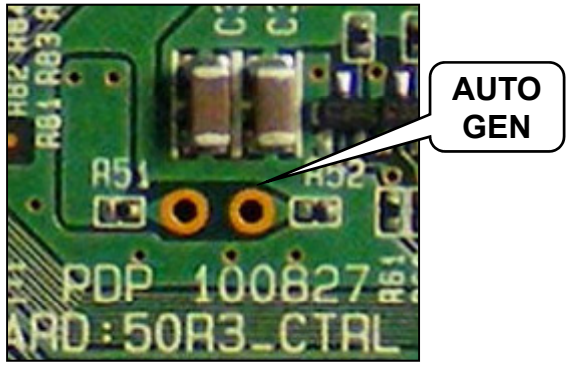
Control Board TP Tips

EXTERNAL TRIGGER: (VS_DA) can be used as an External Trigger for your scope when locking onto the Y-Scan or the Z-Drive signal.





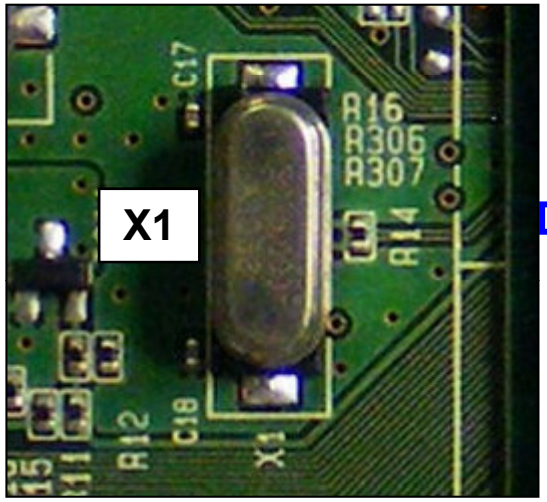


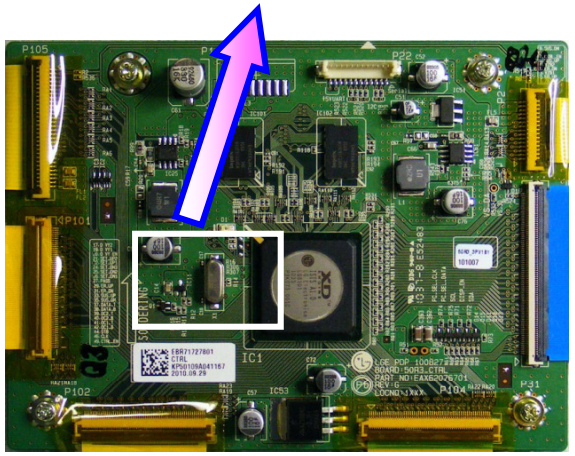


Auto Gen (Internal Automatic Generator)
Short these two pins together to generate patterns on the screen for a Panel Test.
If patterns do not appear, try removing the LVDS Cable.

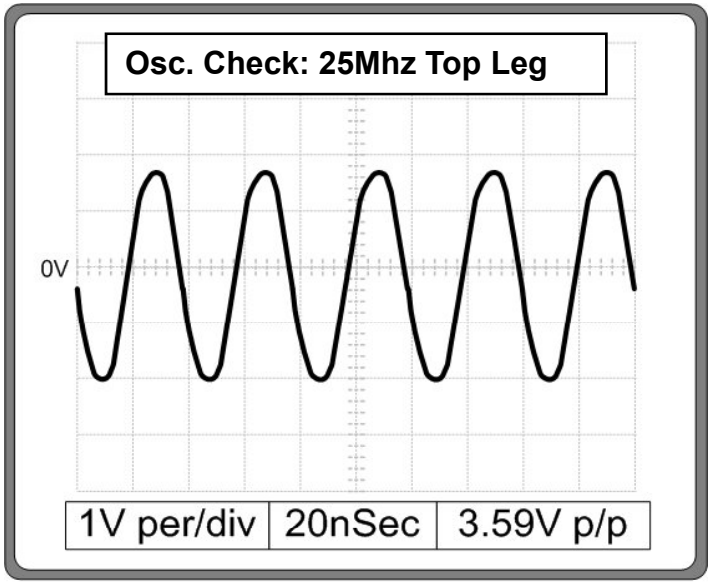
Checking the Crystal X1 "Clock" on the Control Board

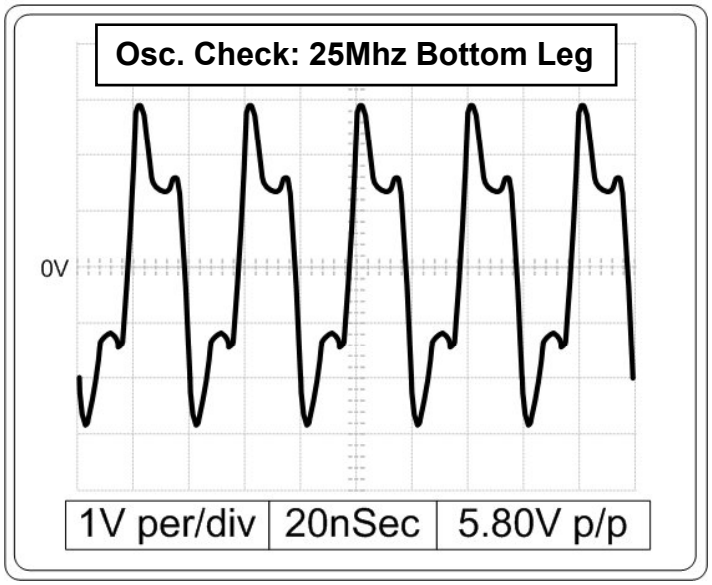
Check the output of the Oscillator (Crystal) X1.
The frequency of the sine wave is 25 MHZ.
Missing this clock signal will halt operation of the panel drive signals.





CONTROL BOARD CRYSTAL LOCATION





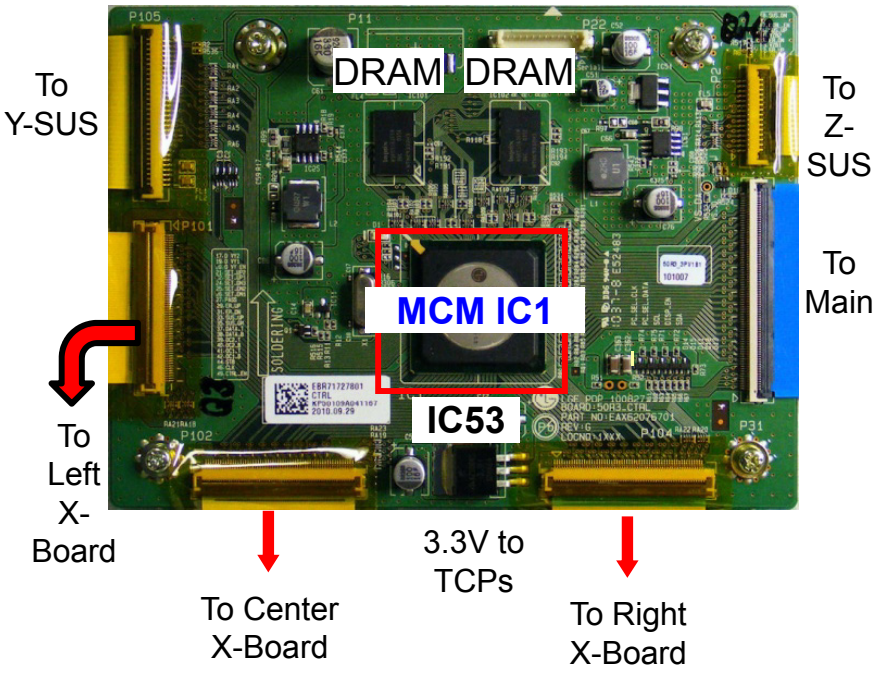
Control Board Signal (Simplified Block Diagram)

The Control Board supplies Video Signals to the TCP (Taped Carrier Package) ICs.

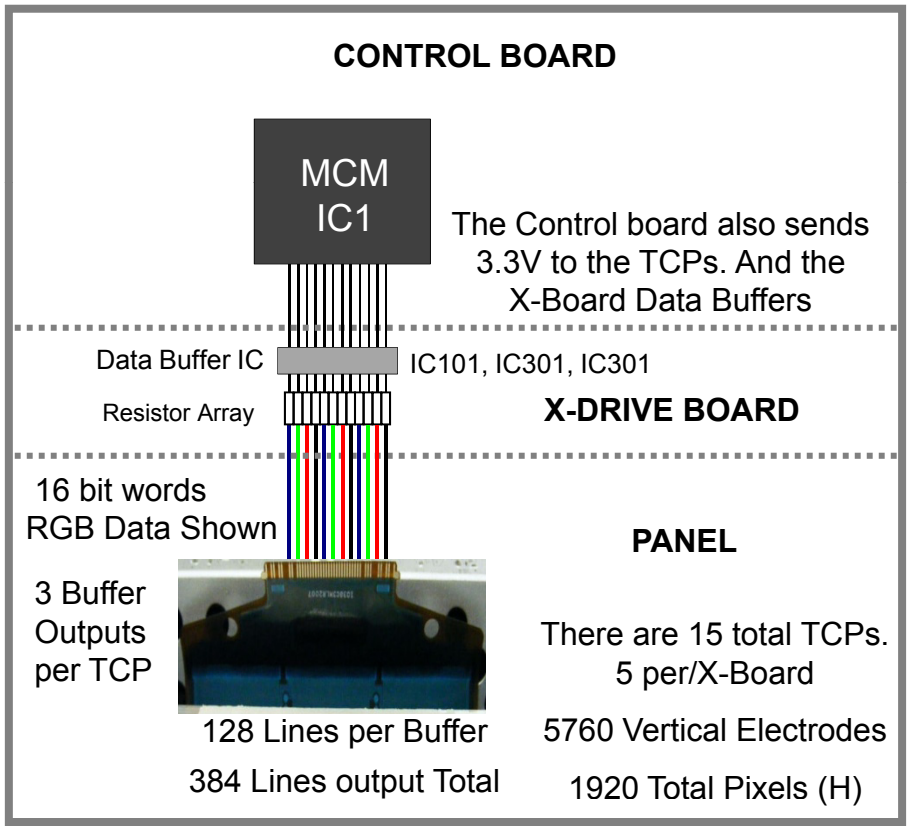
If there is a bar defect on the screen, it could be a Control Board problem.

Control Board to X Board Address Signal Flow

This Picture shows Signal Flow Distribution to help determine the failure depending on where the problem appears on the screen.



Basic Diagram of Control Board



Control Board Connector P105 to Y-SUS P102 Information

Pins are very close together. Use Caution when taking Voltage measurements.

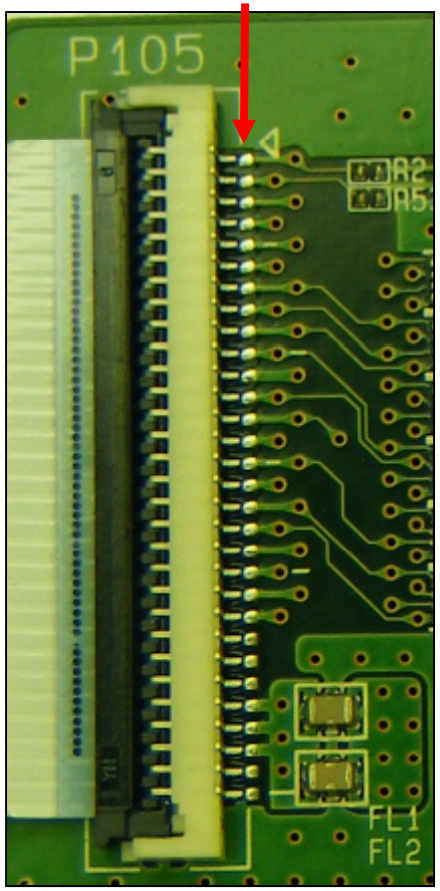
All the rest are delivering Y-SUS Waveform development and Y-Drive logic signals to the Y-SUS Board.

Y-Drive logic signals are simply routed right through the Y-SUS to the Y-Drive boards.

Pins 23 through 25
Receive 18V from the Y-SUS.

Pins 26 through 28
Receive M5V from the Y-SUS.

Pin ①



Note: The +18V is not used by the Control board, it is routed to the Z-SUS leaving on P2 Pins 14~15.

P105 Label Silk Screen

Note: This silk screen and the actual pin function are not correct.
See P105 Connector Voltages and Diode Check from more details.

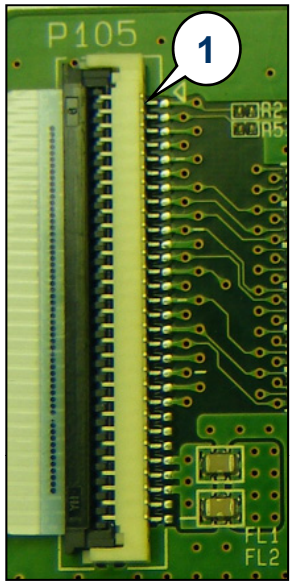
Control P105 to Y-SUS P102 Plug Information

Pin 1 on Control is Pin 50 on Y-SUS.
Note: There are no voltages in Stand-By mode

P105 "Control" to P102 "Y-SUS"

Pin	Label	Run	Diode Check
1	CTRL_OE	0.06V	2.84V
2	OE	0.02V	2.84V
3	SUS_UP	0.13V	2.82V
4	SUS_DN	2.84V	2.83V
5	SET_DN	2.2V	2.82V
6	Slope_Rate_Sel	0.05V	2.82V
7	Det_Level_Sel	0.3V	2.82V
8	Ramp_Slope_Opt	0.06V	2.81V
9	SET_UP	0.06V	2.82V
10	ER_UP	0.11V	2.81V
11	Gnd	Gnd	Gnd
12	ER_DN	0.09V	2.81V
13	BLOCKING	1.02V	2.84V
14	DELTA_VY_O	0.35V	2.81V
15	OC2_TOP	1.98V	2.84V

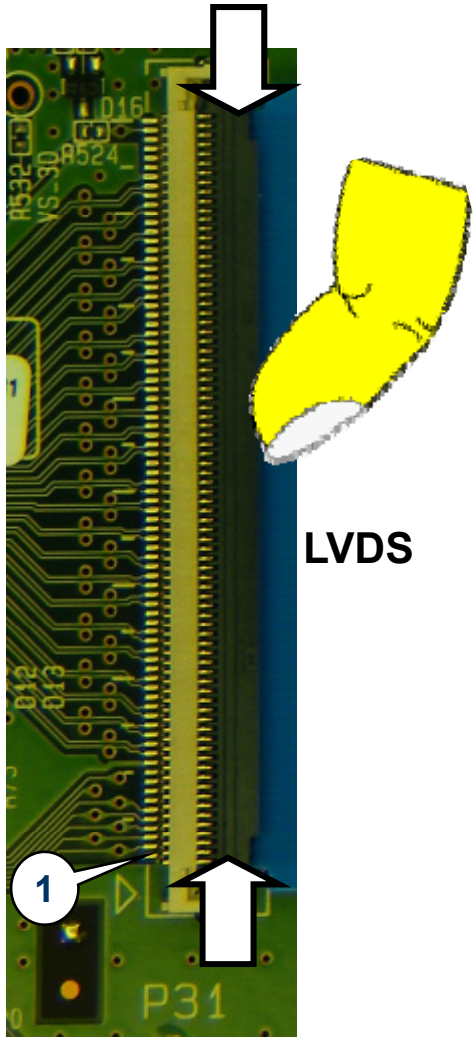
Pin	Label	Run	Diode Check
16	DATA_TOP	0V	2.81V
17	OC1_TOP	1.16V	2.84V
18	CLK	0.46V	Gnd
19	STB	2.86V	Gnd
20	OC1_BTM	Gnd	Gnd
21	DATA_BTM	0V	Gnd
22	OC2_BTM	1.98V	2.98V
23	**+18V**	**18.34V**	**Open**
24	**+18V**	**18.34V**	**Open**
25	**+18V**	**18.34V**	**Open**
26	**M5V**	**4.89V**	**Open**
27	**M5V**	**4.89V**	**Open**
28	**M5V**	**4.89V**	**Open**
29	Gnd	Gnd	Gnd
30	Gnd	Gnd	Gnd



Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

Control Board LVDS P31 Signals

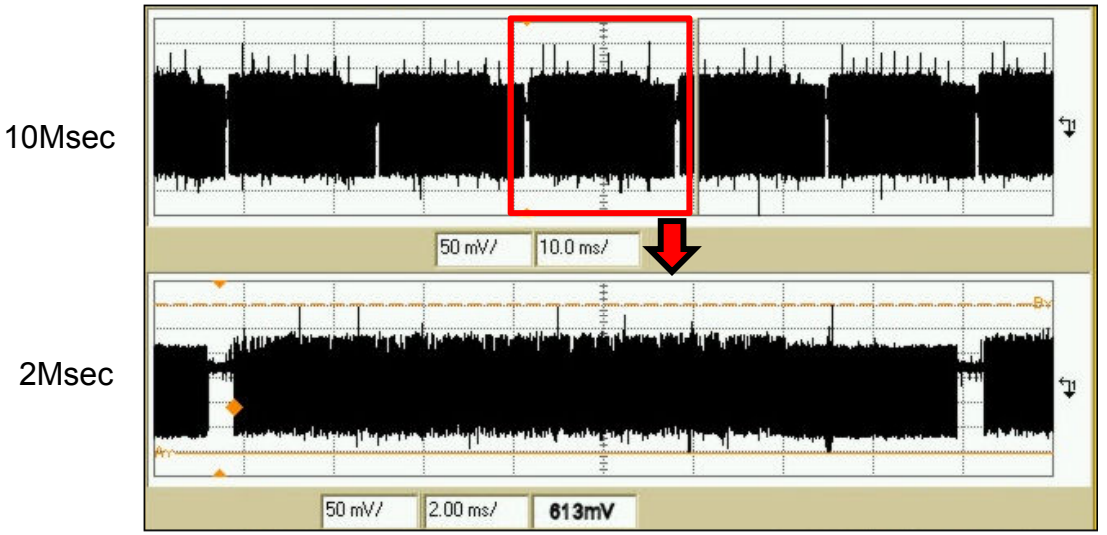
LVDS Cable P31 on Control board shown.
Flip up the locking mechanism to unlock.



Pins are close together.

Video Signals from the Main Board to the Control Board are referred to as Low Voltage Differential Signals or LVDS. The video is delivered in dual 24 bit LVDS format. Their presence can be confirmed with the Oscilloscope by monitoring the LVDS signals with SMPTE Color Bar input. Loss of these Signals would confirm the failure is on the Main Board or the LVDS Cable itself.

Example of LVDS Video Signal (613mV p/p)



Example of Normal Signals measured at 100mV per/div

Pins 12~17, 22~25, 28~33, 38~41, 44~49, 60~65, 70~73 are video.
Pins 19~20, 35~36, 51~52, 67~68 are Clock signals for synchronizing.

Pin 79 is active high when the set is placed into 3D mode.

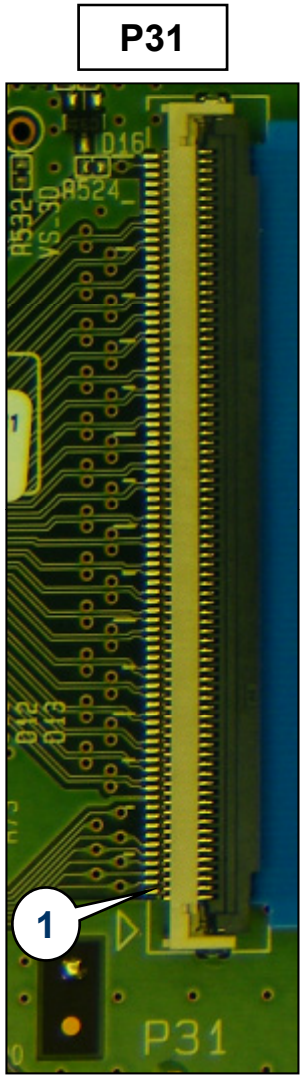
Control Board LVDS P31 Connector Voltages and Diode Check

P31 LVDS "Control" to P701 "Main"

Pin	Label	Run	Diode Check
80	Gnd	Gnd	Gnd
79	n/c	n/c	2.23V
78	ROM_RX	3.3V	3.11V
77	ROM_TX	3.3V	3.11V
76	n/c	n/c	n/c
75	n/c	n/c	n/c
74	Gnd	Gnd	Gnd
73	n/c	n/c	1.05V
72	n/c	n/c	1.05V
71	n/c	n/c	1.05V
70	n/c	n/c	1.05V
69	Gnd	Gnd	Gnd
68	n/c	n/c	1.05V
67	n/c	n/c	1.05V
66	Gnd	Gnd	Gnd
65	n/c	n/c	1.05V
64	n/c	n/c	1.05V
63	n/c	n/c	1.05V
62	n/c	n/c	1.05V
61	n/c	n/c	1.05V
60	n/c	n/c	1.05V
59	Gnd	Gnd	Gnd
58	Gnd	Gnd	Gnd
57	n/c	n/c	1.05V
56	n/c	n/c	1.05V
55	n/c	n/c	1.05V
54	n/c	n/c	1.05V

Pin	Label	Run	Diode Check
53	Gnd	Gnd	Gnd
52	n/c	n/c	1.05V
51	n/c	n/c	1.05V
50	Gnd	Gnd	Gnd
49	n/c	n/c	1.05V
48	n/c	n/c	1.05V
47	n/c	n/c	1.05V
46	n/c	n/c	1.05V
45	n/c	n/c	1.05V
44	n/c	n/c	1.05V
43	Gnd	Gnd	Gnd
42	Gnd	Gnd	Gnd
41	RA1-	1.11V	1.05V
40	RA1+	1.3V	1.05V
39	RB1-	1.11V	1.05V
38	RB1+	1.3V	1.05V
37	Gnd	Gnd	Gnd
36	RC1-	1.11V	1.05V
35	RC1+	1.3V	1.05V
34	Gnd	Gnd	Gnd
33	RCLK1-	1.2V	1.05V
32	RCLK1-	1.2V	1.05V
31	RD1-	1.11V	1.05V
30	RD1+	1.3V	1.05V
29	RE1-	1.11V	1.05V
28	RE1+	1.3V	1.05V
27	Gnd	Gnd	Gnd

Pin	Label	Run	Diode Check
26	Gnd	Gnd	Gnd
25	RA2-	1.11V	1.05V
24	RA2+	1.3V	1.05V
23	RB2-	1.11V	1.05V
22	RB2+	1.3V	1.05V
21	Gnd	Gnd	Gnd
20	RC2-	1.11V	1.05V
19	RC2+	1.3V	1.05V
18	Gnd	Gnd	Gnd
17	RCLK2-	1.2V	1.05V
16	RCLK2-	1.2V	1.05V
15	RD2-	1.11V	1.05V
14	RD2+	1.3V	1.05V
13	RE2-	1.11V	1.05V
12	RE2+	1.3V	Gnd
11	Gnd	Gnd	Gnd
10	n/c	n/c	n/c
9	n/c	n/c	n/c
8	n/c	n/c	n/c
7	n/c	n/c	n/c
6	Module_SDA1	3.3V	2.55V
5	DISP_EN	2.8V	2.55V
4	Module_SCL1	3.3V	2.55V
3	PC_SER_DATA	3.3V	2.55V
2	PC_SER_CLK	0.5V	2.55V
1	Gnd	Gnd	Gnd



*** Indicates video signal**

Note: There are no voltages in Stand-By mode.

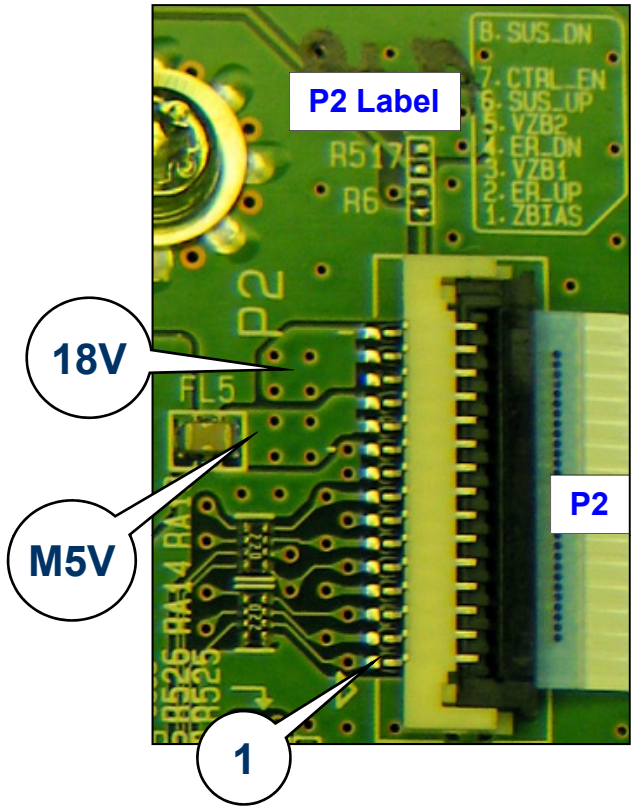
Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

Control Board P2 Connector Pin ID and Voltages

Voltage and Diode Mode Measurements for the Control Board.
Note: There are no voltages in Stand-By mode.

P2 "Control" to "Z-SUS Board" P201

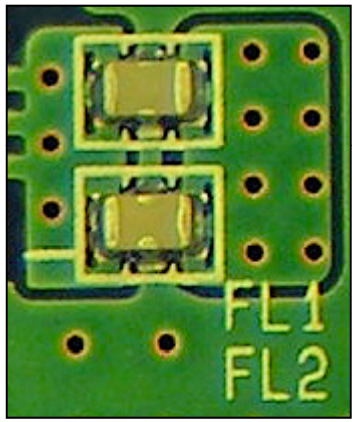
Pin	Label	Run	Diode Check
15	**(+18V)**	**18.34V**	**Open**
14	**(+18V)**	**18.34V**	**Open**
13	n/c	n/c	1.52V
12	**M5V**	**4.89V**	**1.52V**
11	**M5V**	**4.89V**	**1.52V**
10	Gnd	Gnd	Gnd
9	Gnd	Gnd	Gnd
8	SUS_DN	0.73V	Open
7	CTRL_EN	0.06V	Open
6	SUS_UP	0.15V	Open
5	VZB2	2.49V	Open
4	ER_DN	0.1V	Open
3	VZB1	2.53V	Open
2	ER_UP	0.87V	Open
1	ZBIAS	1.9V	Open

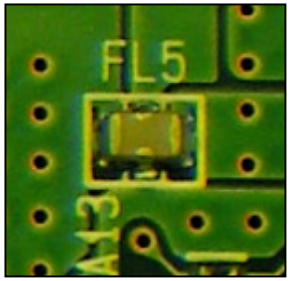


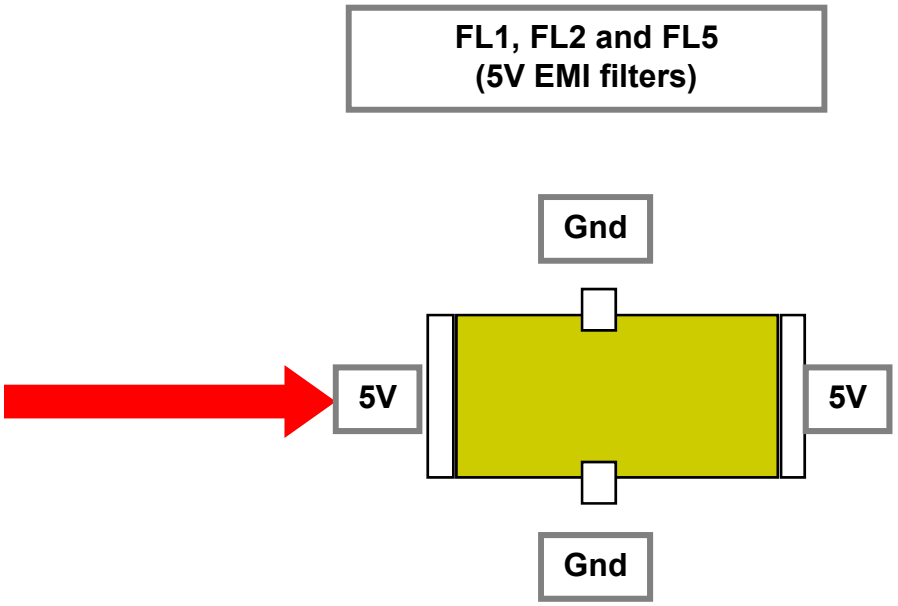
Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

Control Board (EMI Filter) Explained

The two EMI Filters just to the bottom right of P105 and one just to the top left of P2 are surface mount mini devices which shunt high frequencies to ground. These high frequencies are generated on the SMPS, Y-SUS and Control Board.
Each EMI filter has 4 pins as shown in the example.
The left and right are the B+ route, the two side solder points are Chassis Gnd.





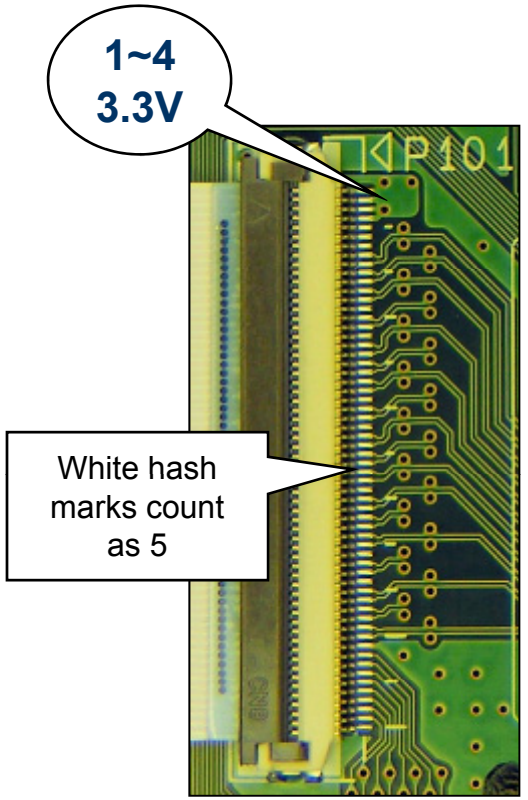


P101 Connector "Control Board" to "Left X Board" P110

P101 "Control" to P110 "X-Left"

Pin	Label	Run	Diode Check
1	3.3V	3.28V	Open
2	3.3V	3.28V	Open
3	3.3V	3.28V	Open
4	3.3V	3.28V	Open
5	n/c	n/c	n/c
6	n/c	n/c	n/c
7	Gnd	Gnd	Gnd
8	TCP1_RSDS_A3N	1.18V	3.09V
9	TCP1_RSDS_A3P	1.25V	3.08V
10	TCP1_RSDS_A2N	1.18V	Open
11	TCP1_RSDS_A2P	1.25V	Open
12	TCP1_RSDS_A1N	1.18V	Gnd
13	TCP1_RSDS_A1P	1.25V	3.09V
14	Gnd	Gnd	Gnd
15	RSDS_CLK_N0	1.34V	1.36V
16	RSDS_CLK_P0	1.08V	1.32V
17	Gnd	Gnd	Gnd
18	TCP2_RSDS_A3N	1.18V	Gnd
19	TCP2_RSDS_A3P	1.25V	1.36V
20	TCP2_RSDS_A2N	1.18V	1.36V
21	TCP2_RSDS_A2P	1.25V	1.36V
22	TCP2_RSDS_A1N	1.18V	1.36V
23	TCP2_RSDS_A1P	1.25V	1.36V
24	Gnd	Gnd	Gnd
25	RSDS_CLK_N1	1.34V	Gnd
26	RSDS_CLK_P1	1.08V	1.36V
27	Gnd	Gnd	Gnd
28	TCP3_RSDS_A3N	1.18V	1.36V
29	TCP3_RSDS_A3P	1.25V	1.32V
30	TCP3_RSDS_A2N	1.18V	Gnd

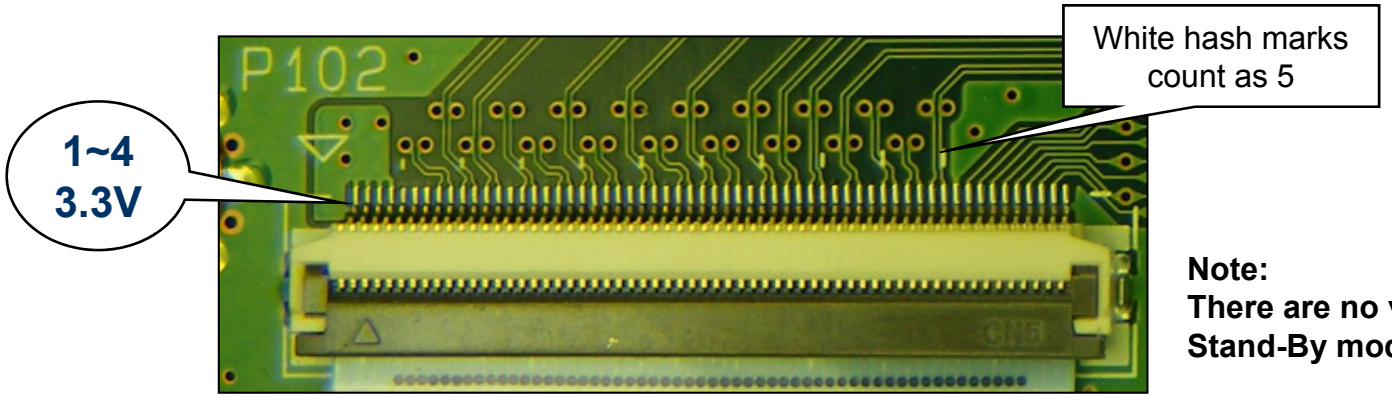
Pin	Label	Run	Diode Check
31	TCP3_RSDS_A2P	1.25V	Open
32	TCP3_RSDS_A1N	1.18V	Open
33	TCP3_RSDS_A1P	1.25V	Open
34	Gnd	Gnd	Gnd
35	TCP4_RSDS_A3N	1.18V	Gnd
36	TCP4_RSDS_A3P	1.25V	1.36V
37	TCP4_RSDS_A2N	1.18V	1.36V
38	TCP4_RSDS_A2P	1.25V	3.09V
39	TCP4_RSDS_A1N	1.18V	3.08V
40	TCP4_RSDS_A1P	1.25V	Open
41	Gnd	Gnd	Gnd
42	RSDS_CLK_N3	1.34V	Gnd
43	RSDS_CLK_P3	1.08V	3.09V
44	Gnd	Gnd	Gnd
45	TCP5_RSDS_A3N	1.18V	1.36V
46	TCP5_RSDS_A3P	1.25V	1.32V
47	TCP5_RSDS_A2N	1.18V	Gnd
48	TCP5_RSDS_A2P	1.25V	Gnd
49	TCP5_RSDS_A1N	1.18V	1.36V
50	TCP5_RSDS_A1P	1.25V	1.36V
51	Gnd	Gnd	Gnd
52	STB0	3.2V	1.36V
53	STB1	3.2V	1.36V
54	X_ER_DN0	0.42V	1.32V
55	X_SUS_DN0	0.42V	Gnd
56	CE1_0	0.42V	1.36V
57	CE2_0	0.42V	1.36V
58	P0C0	1.89V	1.36V
59	BLK0	1.89V	1.32V
60	Gnd	Gnd	Gnd



Note:
There are no voltages in Stand-By mode.

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

P102 Connector "Control Board" to "Center X Board" P310



Note:
There are no voltages in Stand-By mode.

P102 "Control" to P310 "X-Cent"

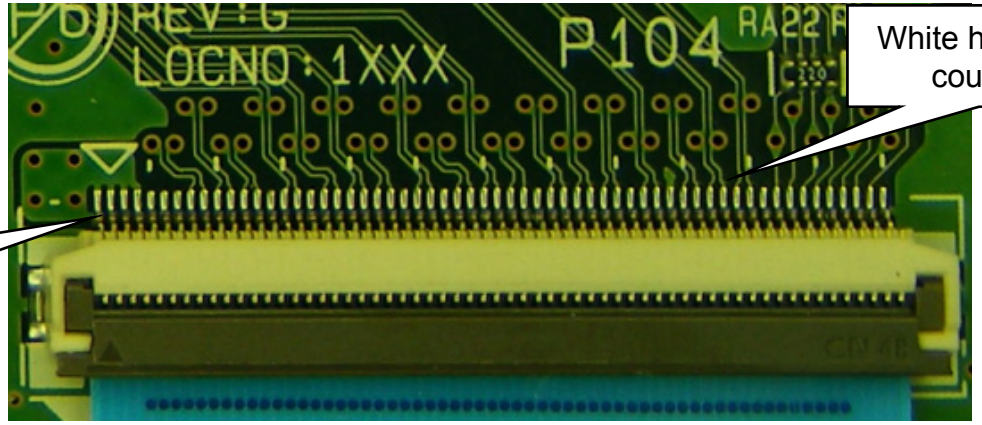
Pin	Label	Run	Diode Check
1	3.3V	3.28V	Open
2	3.3V	3.28V	Open
3	3.3V	3.28V	Open
4	3.3V	3.28V	Open
5	n/c	n/c	n/c
6	n/c	n/c	n/c
7	Gnd	Gnd	Gnd
8	TCP6_RSDS_A3N	1.18V	3.09V
9	TCP6_RSDS_A3P	1.25V	3.08V
10	TCP6_RSDS_A2N	1.18V	Open
11	TCP6_RSDS_A2P	1.25V	Open
12	TCP6_RSDS_A1N	1.18V	Gnd
13	TCP6_RSDS_A1P	1.25V	3.09V
14	Gnd	Gnd	Gnd
15	RSDS_CLK_N0	1.34V	1.36V
16	RSDS_CLK_P0	1.08V	1.32V
17	Gnd	Gnd	Gnd
18	TCP7_RSDS_A3N	1.18V	Gnd
19	TCP7_RSDS_A3P	1.25V	1.36V
20	TCP7_RSDS_A2N	1.18V	1.36V

Pin	Label	Run	Diode Check
21	TCP7_RSDS_A2P	1.25V	1.36V
22	TCP7_RSDS_A1N	1.18V	1.36V
23	TCP7_RSDS_A1P	1.25V	1.36V
24	Gnd	Gnd	Gnd
25	RSDS_CLK_N1	1.34V	Gnd
26	RSDS_CLK_P1	1.08V	1.36V
27	Gnd	Gnd	Gnd
28	TCP8_RSDS_A3N	1.18V	1.36V
29	TCP8_RSDS_A3P	1.25V	1.32V
30	TCP8_RSDS_A2N	1.18V	Gnd
31	TCP8_RSDS_A2P	1.25V	Open
32	TCP8_RSDS_A1N	1.18V	Open
33	TCP8_RSDS_A1P	1.25V	Open
34	Gnd	Gnd	Gnd
35	TCP9_RSDS_A3N	1.18V	Gnd
36	TCP9_RSDS_A3P	1.25V	1.36V
37	TCP9_RSDS_A2N	1.18V	1.36V
38	TCP9_RSDS_A2P	1.25V	3.09V
39	TCP9_RSDS_A1N	1.18V	3.08V
40	TCP9_RSDS_A1P	1.25V	Open

Pin	Label	Run	Diode Check
41	Gnd	Gnd	Gnd
42	RSDS_CLK_N3	1.34V	Gnd
43	RSDS_CLK_P3	1.08V	3.09V
44	Gnd	Gnd	Gnd
45	TCP10_RSDS_A3N	1.18V	1.36V
46	TCP10_RSDS_A3P	1.25V	1.32V
47	TCP10_RSDS_A2N	1.18V	Gnd
48	TCP10_RSDS_A2P	1.25V	Gnd
49	TCP10_RSDS_A1N	1.18V	1.36V
50	TCP10_RSDS_A1P	1.25V	1.36V
51	Gnd	Gnd	Gnd
52	STB4	3.2V	1.36V
53	STB5	3.2V	1.36V
54	X_ER_DN2	0.42V	1.32V
55	X_SUS_DN2	0.42V	Gnd
56	CE1_2	0.42V	1.36V
57	CE2_2	0.42V	1.36V
58	P0C1	1.89V	1.36V
59	BLK1	1.89V	1.32V
60	Gnd	Gnd	Gnd

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

P104 Connector "Control Board" to "Right X Board" P310



Note:
There are no voltages in Stand-By mode.

P104 "Control" to P310 "X-Right"

Pin	Label	Run	Diode Check
1	3.3V	3.28V	Open
2	3.3V	3.28V	Open
3	3.3V	3.28V	Open
4	3.3V	3.28V	Open
5	n/c	n/c	n/c
6	n/c	n/c	n/c
7	Gnd	Gnd	Gnd
8	TCP11_RSDS_A3N	1.18V	3.09V
9	TCP11_RSDS_A3P	1.25V	3.08V
10	TCP11_RSDS_A2N	1.18V	Open
11	TCP11_RSDS_A2P	1.25V	Open
12	TCP11_RSDS_A1N	1.18V	Gnd
13	TCP11_RSDS_A1P	1.25V	3.09V
14	Gnd	Gnd	Gnd
15	RSDS_CLK_NB	1.34V	1.36V
16	RSDS_CLK_PB	1.08V	1.32V
17	Gnd	Gnd	Gnd
18	TCP12_RSDS_A3N	1.18V	Gnd
19	TCP12_RSDS_A3P	1.25V	1.36V
20	TCP12_RSDS_A2N	1.18V	1.36V

Pin	Label	Run	Diode Check
21	TCP12_RSDS_A2P	1.25V	1.36V
22	TCP12_RSDS_A1N	1.18V	1.36V
23	TCP12_RSDS_A1P	1.25V	1.36V
24	Gnd	Gnd	Gnd
25	RSDS_CLK_N9	1.34V	Gnd
26	RSDS_CLK_P9	1.08V	1.36V
27	Gnd	Gnd	Gnd
28	TCP13_RSDS_A3N	1.18V	1.36V
29	TCP13_RSDS_A3P	1.25V	1.32V
30	TCP13_RSDS_A2N	1.18V	Gnd
31	TCP13_RSDS_A2P	1.25V	Open
32	TCP13_RSDS_A1N	1.18V	Open
33	TCP13_RSDS_A1P	1.25V	Open
34	Gnd	Gnd	Gnd
35	TCP14_RSDS_A3N	1.18V	Gnd
36	TCP14_RSDS_A3P	1.25V	1.36V
37	TCP14_RSDS_A2N	1.18V	1.36V
38	TCP14_RSDS_A2P	1.25V	3.09V
39	TCP14_RSDS_A1N	1.18V	3.08V
40	TCP14_RSDS_A1P	1.25V	Open

Pin	Label	Run	Diode Check
41	Gnd	Gnd	Gnd
42	RSDS_CLK_N11	1.34V	Gnd
43	RSDS_CLK_P11	1.08V	3.09V
44	Gnd	Gnd	Gnd
45	TCP15_RSDS_A3N	1.18V	1.36V
46	TCP15_RSDS_A3P	1.25V	1.32V
47	TCP15_RSDS_A2N	1.18V	Gnd
48	TCP15_RSDS_A2P	1.25V	Gnd
49	TCP15_RSDS_A1N	1.18V	1.36V
50	TCP15_RSDS_A1P	1.25V	1.36V
51	Gnd	Gnd	Gnd
52	STB4	3.2V	1.36V
53	STB5	3.2V	1.36V
54	X_ER_DN2	0.42V	1.32V
55	X_SUS_DN2	0.42V	Gnd
56	CE1_2	0.42V	1.36V
57	CE2_2	0.42V	1.36V
58	P0C1	1.89V	1.36V
59	BLK1	1.89V	1.32V
60	Gnd	Gnd	Gnd

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

X BOARD (LEFT, RIGHT and CENTER) SECTION

The following section gives detailed information about the X boards. These boards deliver the Color information signal developed on the Control board to the TCPs, (Taped Carrier Packages). The TCPs are attached to the vertical FPCs, (Flexible Printed Circuits) which are attached directly to the panel. The X boards are the attachment points for these FPCs.
These boards have no adjustment.

The X-Boards receive their main B+ from:

Originally developed on the Switch Mode Power Supply Va (Voltage for Address) is routed through the Y-SUS board and then to the Left X board via P203 pins 4~5. Va also leaves P120 and is sent to the Center X via P320 pins 1~2. Then it leaves on P321 and goes to the Right X P320 pins 1~2.

Control board develops 3.3V (IC53) and routes to each X-Board via ribbon connectors P110, P310 and P310.

X Board Additional Information

There are three X boards, the Left, Center and the Right (As viewed from the rear of the set).

The three X boards have very little circuitry, primarily a Data Buffer and some passive voltage dividers. They are basically signal and voltage routing boards.

- **They route Va voltage to all of the Taped Carrier Packages (TCPs). Va is introduced to the Left X board first, then the Left X sends Va to the Center X and then the Center X sends Va to the Right X.**
- **They route the Logic (Color) signals from the Control board to all of the Taped Carrier Packages (TCPs).**
- **The X boards have connectors to 15 TCPs, 5 on each X-Board.**

There are a total of 15 TCPs and each TCP has 3 internal buffers, each buffer output 128 pins to the vertical electrodes. So there are a total of 45 buffers feeding the panel's 5760 vertical electrodes.

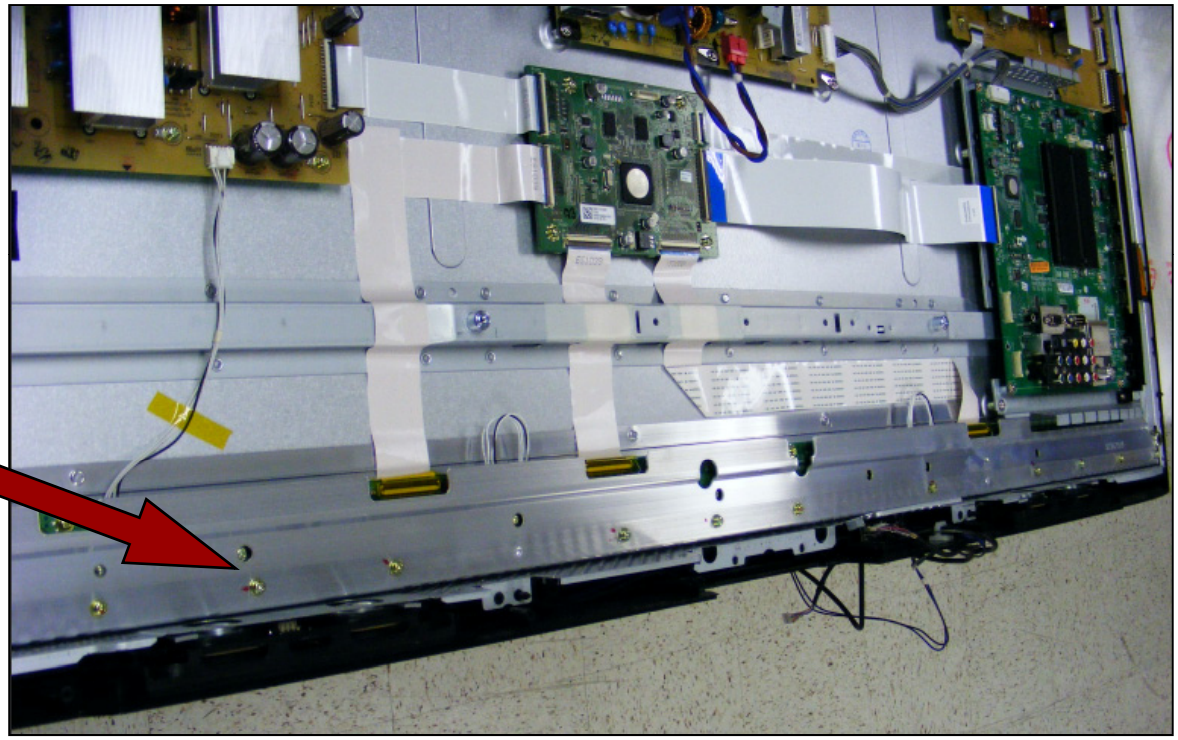
Divide 5760 by 3 to determine the horizontal resolution of the panel (1920).

X Board TCP Heat Sink Warning

NEVER run the television with this heat sink removed. Damage to the TCPs will occur and cause a defective panel.

The Vertical Address buffers (TCPs) have one heat sink indicated by the arrow.

It protects all 15 TCPs.



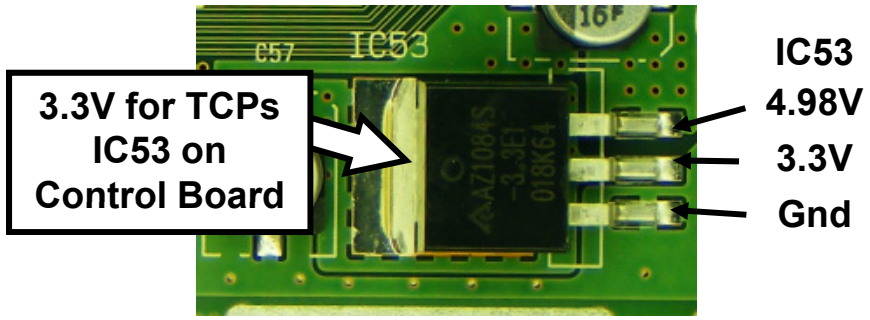
TCP 3.3V B+ Check

Warning: DO NOT attempt to run the set with the Heat Sink over the TCPs removed.

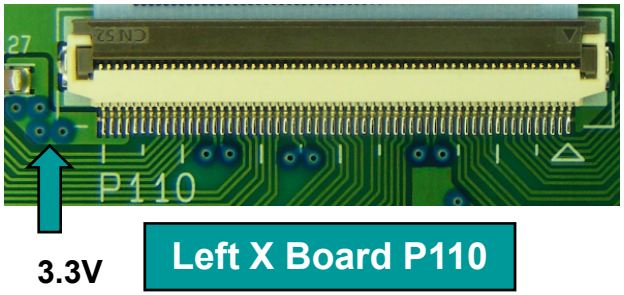
For Connectors P101, P102 and P104 on the Control board, see Control board section. 3.3V leaves on Pins 1~4 of all three connectors.

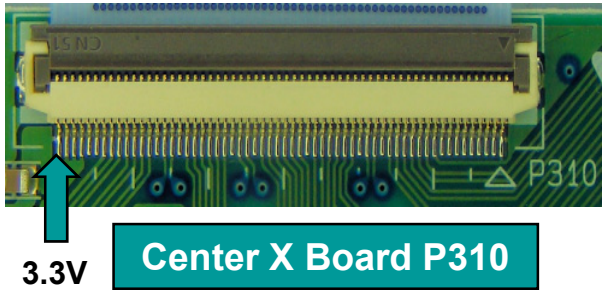
With all connectors connected, place the Red Lead On 3.3V Diode Check (0.62V) Black Lead On 3.3V Diode Check (0.33V) This also test Data ICs on X-Boards

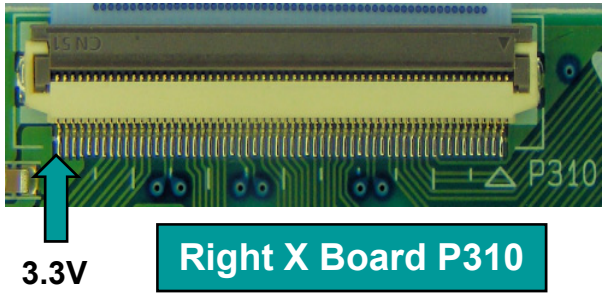
Checking IC53 for 3.3V, use center pin or Top of component.

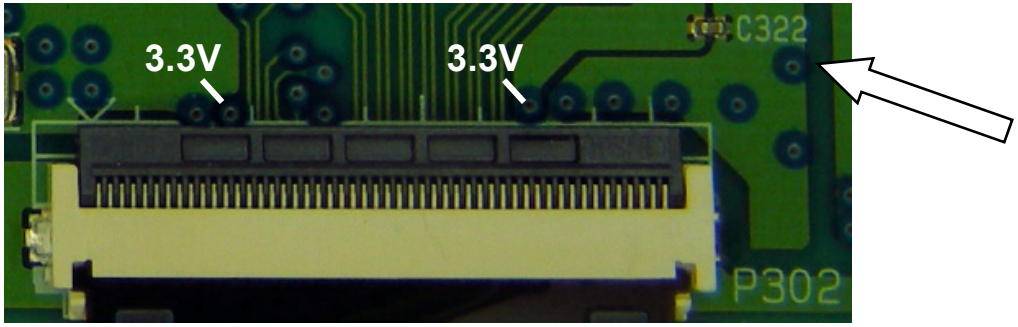


3.3V in on Pins 57 ~ 60 on any connector from the Control board





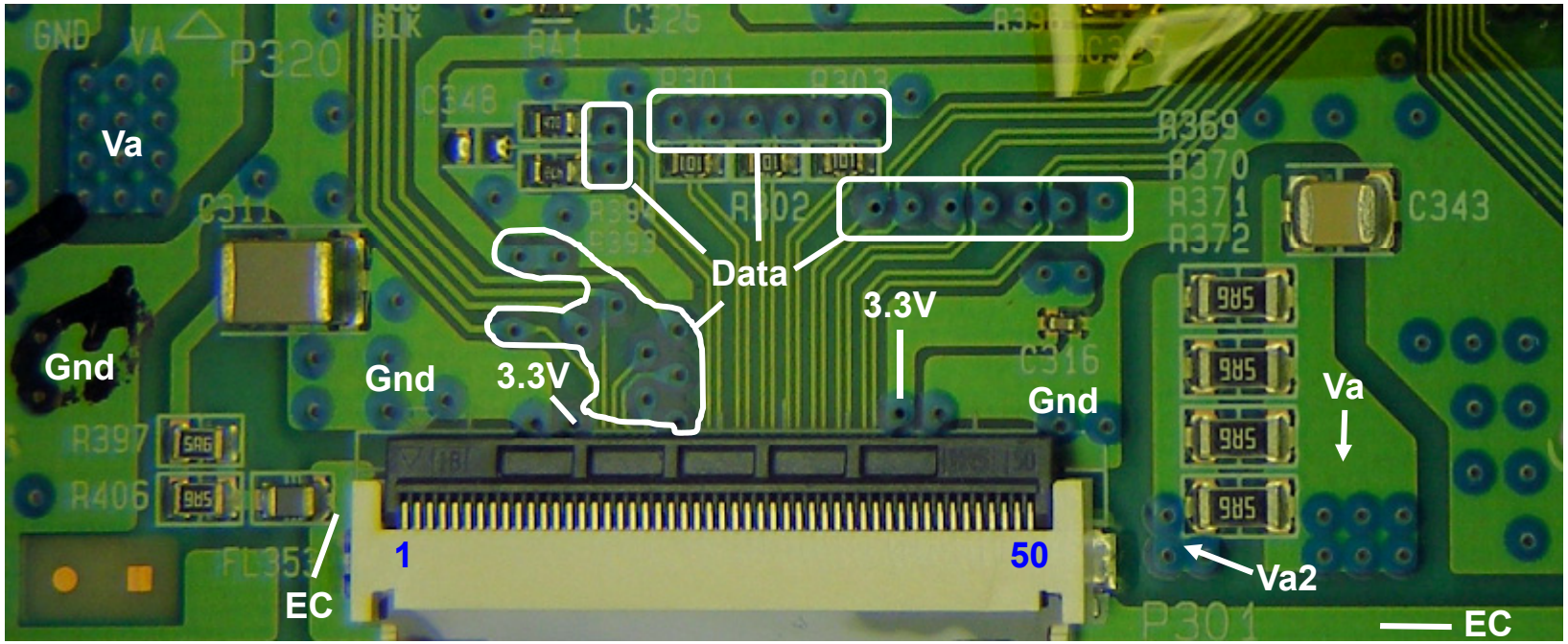




All Connectors to All TCPs look very similar for the 3.3V test point. The trace at pins 14 and 38 of each connector. There will a small feed trough off pin 14 and 38 you can use for Test Points. Example here from P302. You can also note a Capacitor (C322 here) left side to identify Pin 38. You can only check for continuity back to IC53, you can not run the set with heat sink removed, unless you disconnect VA from the Y-SUS to the Left X-Board.

X Board Layout Primary Circuit Diode Check

The three X-Boards have similar circuit layouts for the connections going to the TCPs, as shown below.



Testing a single X board. Disconnected for any other board.

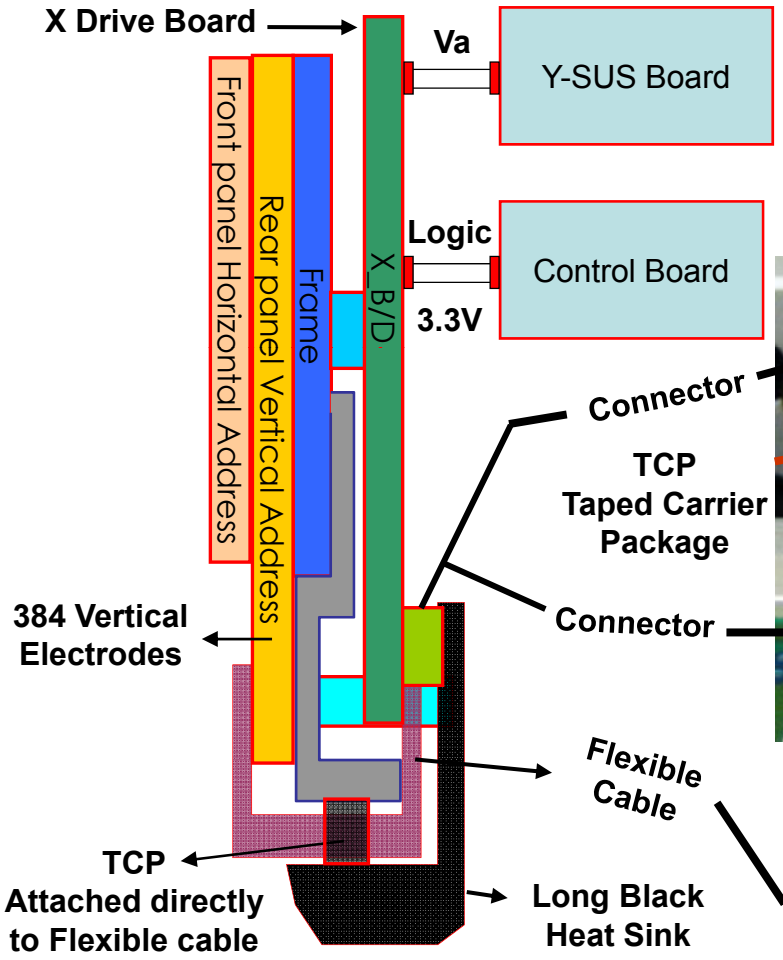
All TCPs Connected	**All TCPs Disconnected**
Red Lead On 3.3V Diode Check (Open)	**Red Lead On 3.3V Diode Check (Open)**
Black Lead On 3.3V Diode Check (0.38V)	**Black Lead On 3.3V Diode Check (0.58V)**
This also test Data ICs on X-Boards.	**This test the Data IC on X-Board.**

To Test EC. Do not run the set with the heat sink removed. Disconnect VA from all X-Boards by disconnecting Y-SUS. EC reads 27.76V. EC Diode Test: Red Lead on EC (Open). Black lead on EC (Open). TCPs connected or disconnected.

VA test: Explained on page 131.

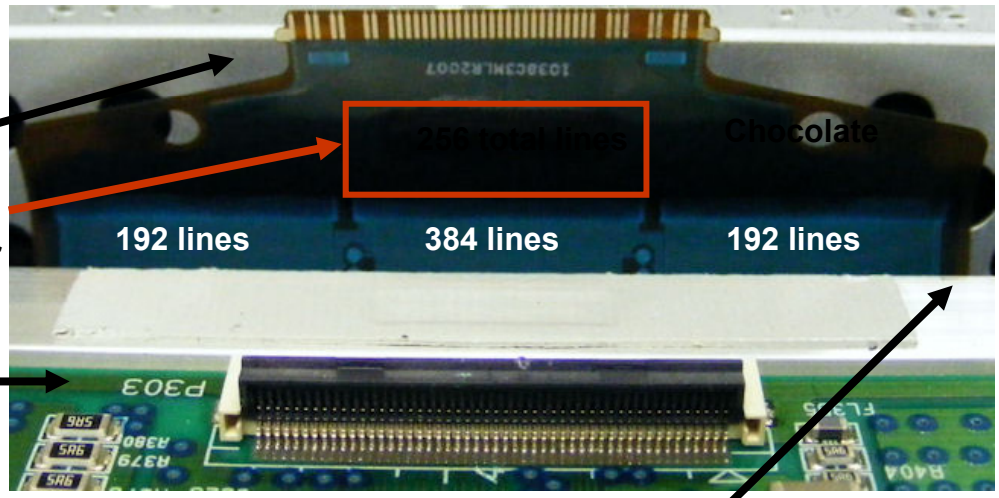
TCP (Tape Carrier Package)

This shows the layout of the bottom ribbon cables connecting to the Panel's Vertical electrodes, (Address Bus). Note that each ribbon cable has a solid state device called a TCP attached.



New Type of TCP

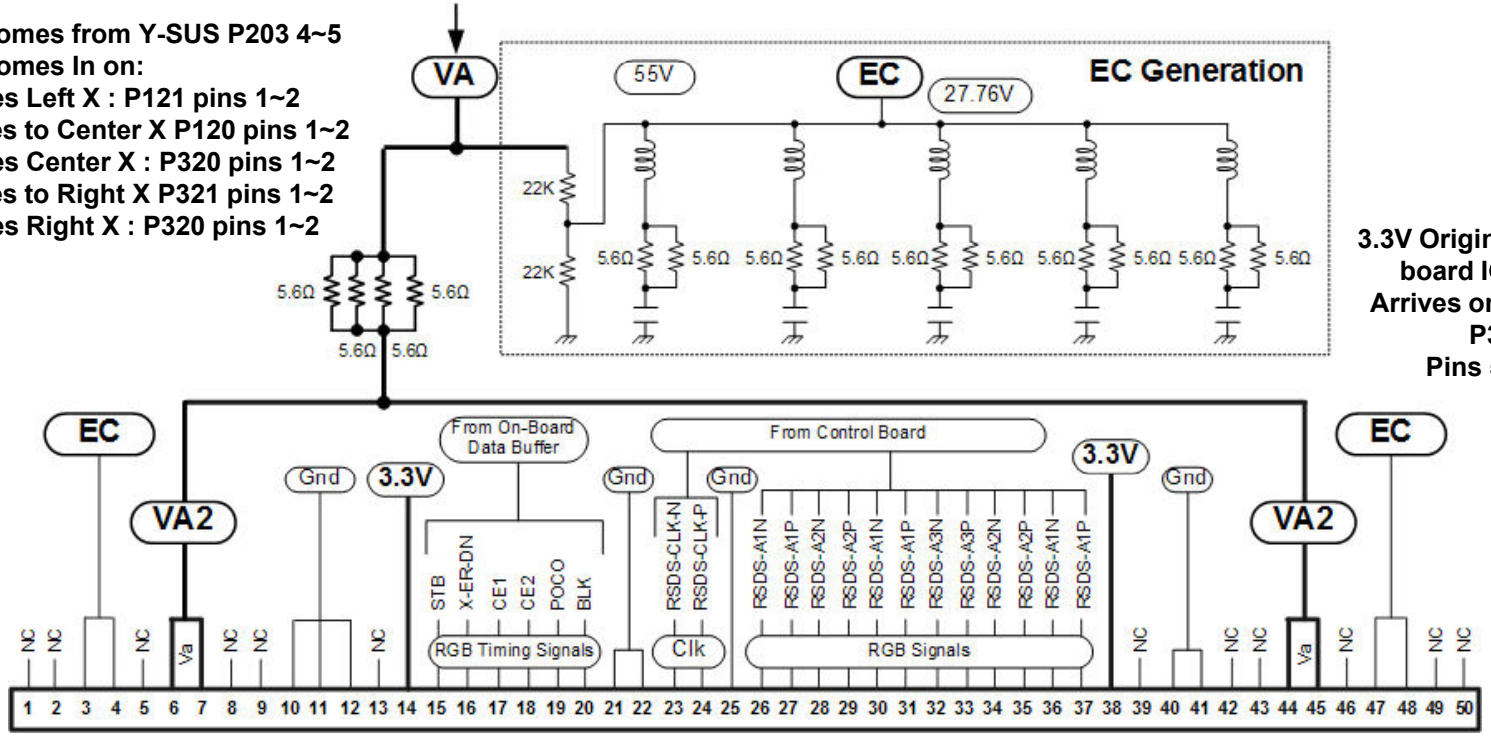
Back side of TCP Ribbon



TCP Testing

50PV450 X Board TCP Connector Distribution
Any X Board to Any TCP (L) P101~P105 or (C) P201~P205 or (R) P201~P305

Va: Comes from Y-SUS P203 4~5
Va: Comes In on:
Arrives Left X : P121 pins 1~2
Leaves to Center X P120 pins 1~2
Arrives Center X : P320 pins 1~2
Leaves to Right X P321 pins 1~2
Arrives Right X : P320 pins 1~2



3.3V Originates from Control board IC53 center leg.
Arrives on X boards P110, P310, P310
Pins 57, 58, 59, 60

On Va (0.42V) **On Va (Open)**

Must be checked on flexible cable.

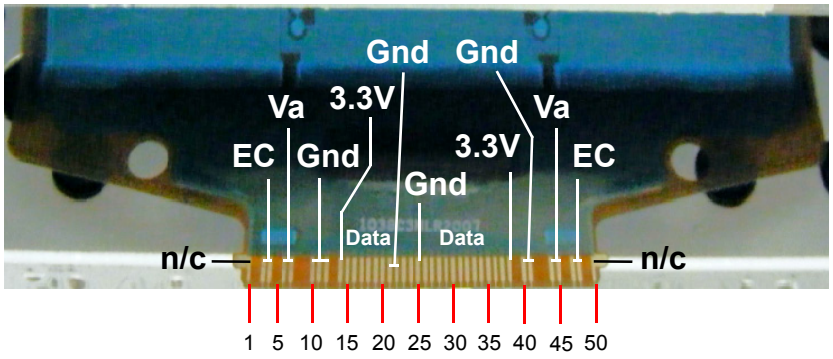
On the below:

On Va2 (0.5V)
On 3.3V (0.44V)
On EC (Open)

On the below:

On Va (Open)
On 3.3V (1.15V)
On EC (Open)

Flexible Printed Ribbon Cable to TCP IC



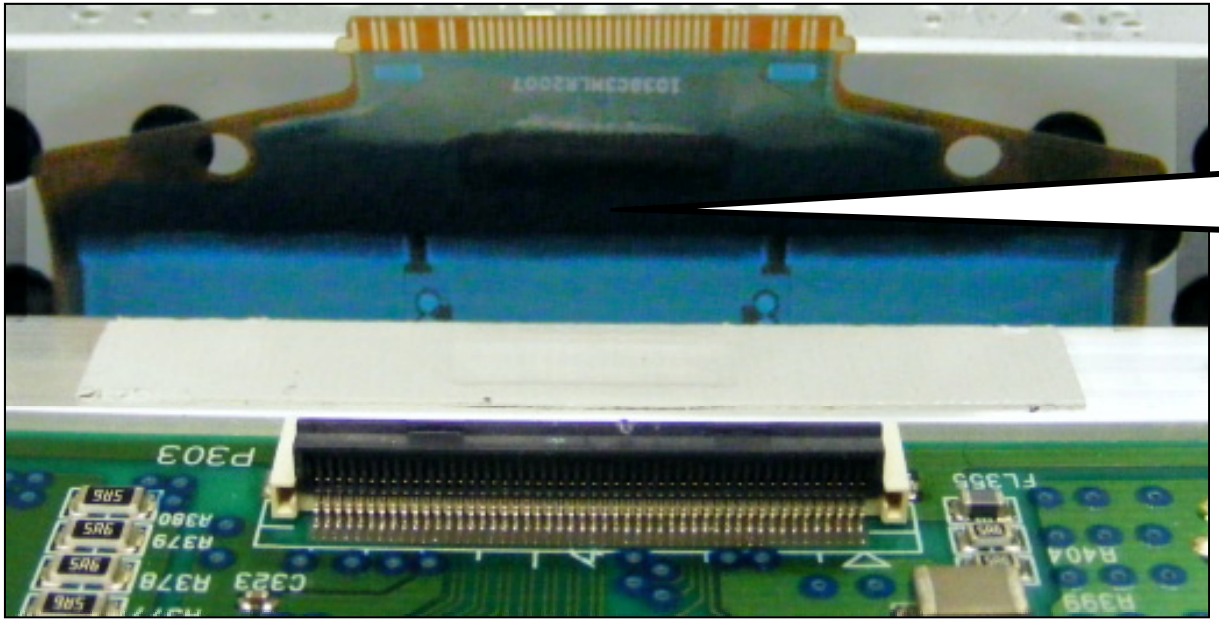
Look for any TCPs being discolored.
Ribbon Damage.
Cracks, folds
Pinches, scratches, etc…

TCP Visual Observation. Damaged TCP

Warning: DO NOT attempt to run the set with the Heat Sink over the TCPs removed. After a very short time, these ICs will begin to self destruct due to overheating.

This damaged TCP can, (at the location of the TCP).

a) Cause the Power Supply to shutdown. (VA shorted, 3.3V shorted).
b) Generate abnormal vertical bars, (colored noise).
c) Cause the entire area driven by the TCP to be "All White" or "ALL BLACK".
d) Cause a "Single Pixel Width Line" defect. The line can be Red, Green or Blue.
e) A dirty contact at the connector can cause b, c and d also.



Look for burns, pin holes, damage, etc.

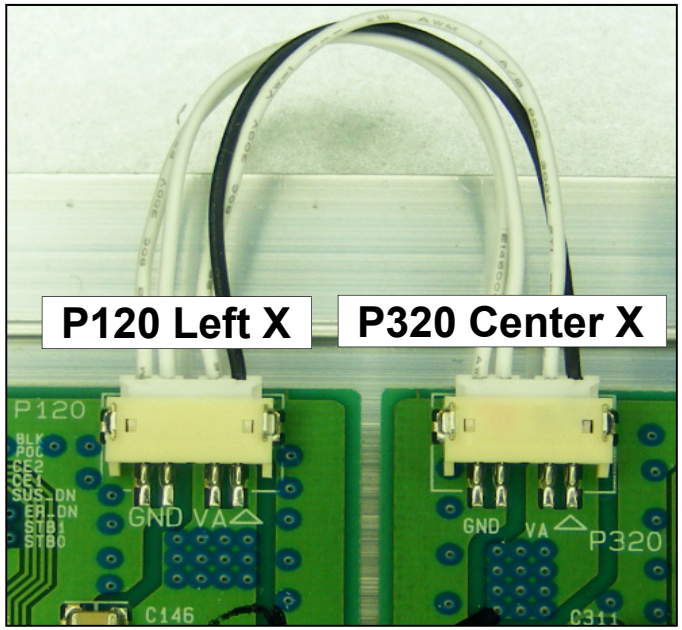
P120, P320, P321 and P320 Connector Va from Left to Center to Right X

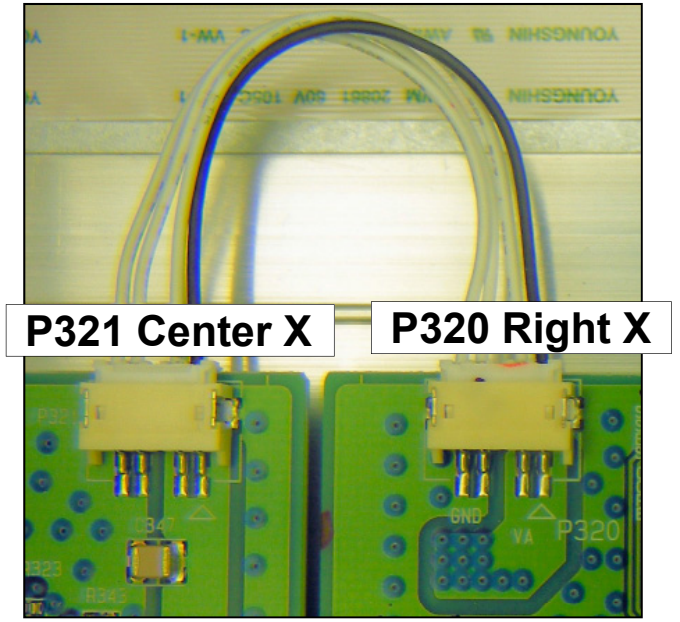
Voltage and Diode Mode Measurement (No Stand-By Voltages)

All Connectors are 4 Pin

Pin	Label	Run	Diode Mode
1-2	VA	*55V	Open
3-4	Gnd	Gnd	Gnd

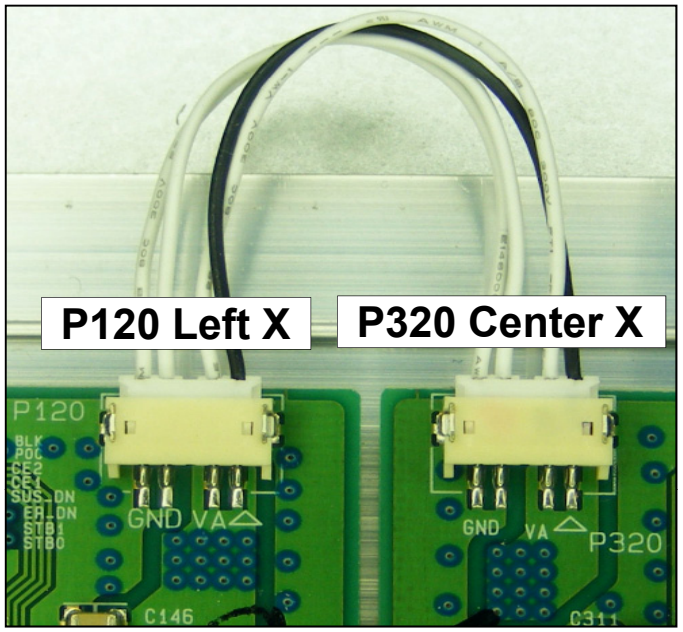
*** Note: This voltage will vary in accordance with Panel Label.**
There are no Stand-By voltages on this connector.





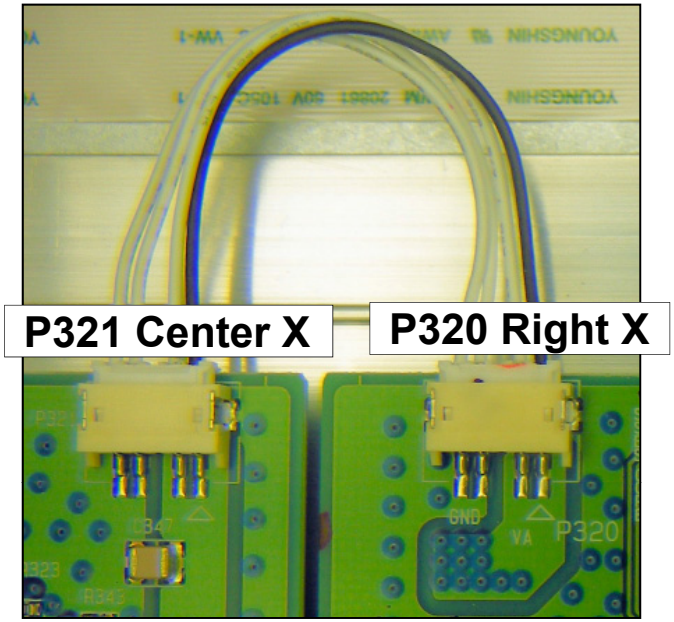
Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

P120, P220, P221 and P320 X Board Connector (VA Diode Check)



Va Right 2 pins
Gnd Left 2 pins

Both Connectors



Va Right 2 pins
Gnd Left 2 pins

Both Connectors

(-) On Chassis Gnd

(+) On Va (Open) all connectors connected.
On Va (Open) Y-SUS connector removed, TCPs connected.
On Va (Open) all connectors removed, TCPs disconnected.

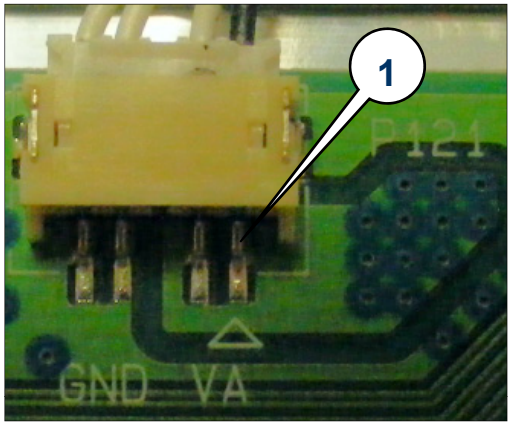
(+) On Chassis Gnd

(-) On Va (0.42) all connectors connected.
On Va (0.42) Y-SUS connector removed, TCPs connected.
On Va (Open) all connectors removed, TCPs disconnected.

P121 Left X Drive Connector from Y-SUS P203 Information

Voltage and Diode Mode Measurement (No Stand-By Voltages)

Heat Sink Removed



P121 Connector " X-Drive Left Board" from "Y-SUS" P203

Pin	Label	Run	Diode Mode
1-2	VA	*55V	Open
3	n/c	n/c	n/c
4-5	Gnd	Gnd	Gnd

*** Note: This voltage will vary in accordance with Panel Label. There are no Stand-By voltages on this connector.**

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

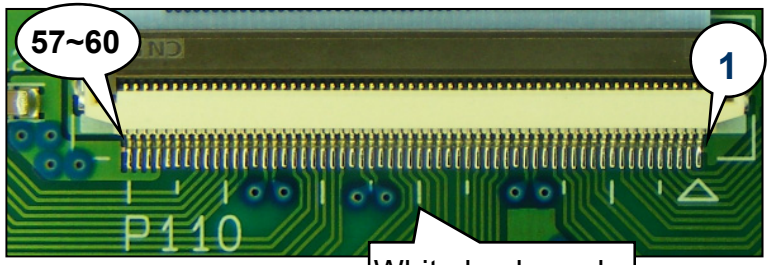
P110 Connector "Left X Board" to "Control" P101

P110 "X-Left" to P101 "Control"

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	BLK0	1.89V	Open
3	P0C0	1.89V	Open
4	CE2_0	0.42V	Open
5	CE1_0	0.42V	Open
6	X_SUS_DN0	0.42V	Open
7	X_ER_DN0	0.42V	Open
8	STB1	3.2V	Open
9	STB0	3.2V	Open
10	Gnd	Gnd	Gnd
11	TCP5_RSDS_A1P	1.25V	Open
12	TCP5_RSDS_A1N	1.18V	Open
13	TCP5_RSDS_A2P	1.25V	Open
14	TCP5_RSDS_A2N	1.18V	Open
15	TCP5_RSDS_A3P	1.25V	Open
16	TCP5_RSDS_A3N	1.18V	Open
17	Gnd	Gnd	Gnd
18	RSDS_CLK_P3	1.08V	Open
19	RSDS_CLK_N3	1.34V	Open
20	Gnd	Gnd	Gnd
21	TCP4_RSDS_A1P	1.25V	Open
22	TCP4_RSDS_A1N	1.18V	Open

Pin	Label	Run	Diode Check
23	TCP4_RSDS_A2P	1.25V	Open
24	TCP4_RSDS_A2N	1.18V	Open
25	TCP4_RSDS_A3P	1.25V	Open
26	TCP4_RSDS_A3N	1.18V	Open
27	Gnd	Gnd	Gnd
28	TCP3_RSDS_A1P	1.25V	Open
29	TCP3_RSDS_A1N	1.18V	Open
30	TCP3_RSDS_A2P	1.25V	Open
31	TCP3_RSDS_A2N	1.18V	Open
32	TCP3_RSDS_A3P	1.25V	Open
33	TCP3_RSDS_A3N	1.18V	Open
34	Gnd	Gnd	Gnd
35	RSDS_CLK_P1	1.08V	Open
36	RSDS_CLK_N1	1.34V	Open
37	Gnd	Gnd	Gnd
38	TCP2_RSDS_A1P	1.25V	Open
39	TCP2_RSDS_A1N	1.18V	Open
40	TCP2_RSDS_A2P	1.25V	Open
41	TCP2_RSDS_A2N	1.18V	Open
42	TCP2_RSDS_A3P	1.25V	Open
43	TCP2_RSDS_A3N	1.18V	Open
44	Gnd	Gnd	Gnd

Pin	Label	Run	Diode Check
45	RSDS_CLK_P0	1.08V	Open
46	RSDS_CLK_N0	1.34V	Open
47	Gnd	Gnd	Gnd
48	TCP1_RSDS_A1P	1.25V	Open
49	TCP1_RSDS_A1N	1.18V	Open
50	TCP1_RSDS_A2P	1.25V	Open
51	TCP1_RSDS_A2N	1.18V	Open
52	TCP1_RSDS_A3P	1.25V	Open
53	TCP1_RSDS_A3N	1.18V	Open
54	Gnd	Gnd	Gnd
55	n/c	n/c	Open
56	n/c	n/c	Open
57	3.3V	3.28V	Open
58	3.3V	3.28V	Open
59	3.3V	3.28V	Open
60	3.3V	3.28V	Open



57~60 pins
3.3V TP

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

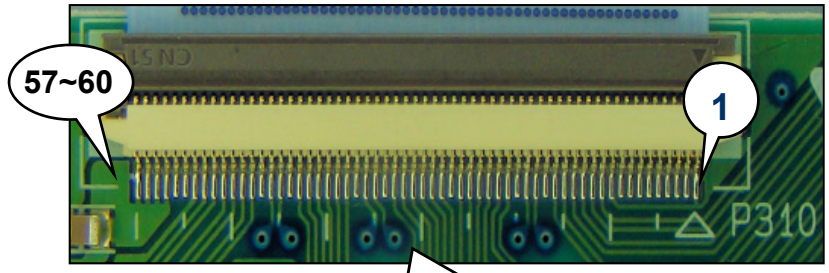
P310 Connector "Center X Board" to "Control Board" P102

P310 "X-Cent" to P102 "Control"

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	BLK1	1.89V	Open
3	P0C1	1.89V	Open
4	CE2_2	0.42V	Open
5	CE1_2	0.42V	Open
6	X_SUS_DN2	0.42V	Open
7	X_ER_DN2	0.42V	Open
8	STB5	3.2V	Open
9	STB4	3.2V	Open
10	Gnd	Gnd	Gnd
11	TCP10_RSDS_A1P	1.25V	Open
12	TCP10_RSDS_A1N	1.18V	Open
13	TCP10_RSDS_A2P	1.25V	Open
14	TCP10_RSDS_A2N	1.18V	Open
15	TCP10_RSDS_A3P	1.25V	Open
16	TCP10_RSDS_A3N	1.18V	Open
17	Gnd	Gnd	Gnd
18	RSDS_CLK_P3	1.08V	Open
19	RSDS_CLK_N3	1.34V	Open
20	Gnd	Gnd	Gnd
21	TCP9_RSDS_A1P	1.25V	Open
22	TCP9_RSDS_A1N	1.18V	Open

Pin	Label	Run	Diode Check
23	TCP9_RSDS_A2P	1.25V	Open
24	TCP9_RSDS_A2N	1.18V	Open
25	TCP9_RSDS_A3P	1.25V	Open
26	TCP9_RSDS_A3N	1.18V	Open
27	Gnd	Gnd	Gnd
28	TCP8_RSDS_A1P	1.25V	Open
29	TCP8_RSDS_A1N	1.18V	Open
30	TCP8_RSDS_A2P	1.25V	Open
31	TCP8_RSDS_A2N	1.18V	Open
32	TCP8_RSDS_A3P	1.25V	Open
33	TCP8_RSDS_A3N	1.18V	Open
34	Gnd	Gnd	Gnd
35	RSDS_CLK_P1	1.08V	Open
36	RSDS_CLK_N1	1.34V	Open
37	Gnd	Gnd	Gnd
38	TCP7_RSDS_A1P	1.25V	Open
39	TCP7_RSDS_A1N	1.18V	Open
40	TCP7_RSDS_A2P	1.25V	Open
41	TCP7_RSDS_A2N	1.18V	Open
42	TCP7_RSDS_A3P	1.25V	Open
43	TCP7_RSDS_A3N	1.18V	Open
44	Gnd	Gnd	Gnd

Pin	Label	Run	Diode Check
45	RSDS_CLK_P0	1.08V	Open
46	RSDS_CLK_N0	1.34V	Open
47	Gnd	Gnd	Gnd
48	TCP6_RSDS_A1P	1.25V	Open
49	TCP6_RSDS_A1N	1.18V	Open
50	TCP6_RSDS_A2P	1.25V	Open
51	TCP6_RSDS_A2N	1.18V	Open
52	TCP6_RSDS_A3P	1.25V	Open
53	TCP6_RSDS_A3N	1.18V	Open
54	Gnd	Gnd	Gnd
55	n/c	n/c	Open
56	n/c	n/c	Open
57	3.3V	3.28V	Open
58	3.3V	3.28V	Open
59	3.3V	3.28V	Open
60	3.3V	3.28V	Open
60	3.3V	3.28V	Open



57~60 pins
3.3V TP

White hash marks count as 5

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

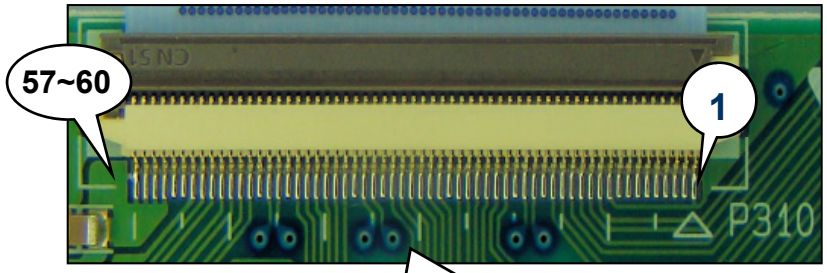
P310 Connector "Right X Board" to "Control" P104

P310 "X-Right" to P104 "Control"

Pin	Label	Run	Diode Check
1	Gnd	Gnd	Gnd
2	BLK1	1.89V	Open
3	P0C1	1.89V	Open
4	CE2_2	0.42V	Open
5	CE1_2	0.42V	Open
6	X_SUS_DN2	0.42V	Open
7	X_ER_DN2	0.42V	Open
8	STB5	3.2V	Open
9	STB4	3.2V	Open
10	Gnd	Gnd	Gnd
11	TCP15_RSDS_A1P	1.25V	Open
12	TCP15_RSDS_A1N	1.18V	Open
13	TCP15_RSDS_A2P	1.25V	Open
14	TCP15_RSDS_A2N	1.18V	Open
15	TCP15_RSDS_A3P	1.25V	Open
16	TCP15_RSDS_A3N	1.18V	Open
17	Gnd	Gnd	Gnd
18	RSDS_CLK_P11	1.08V	Open
19	RSDS_CLK_N11	1.34V	Open
20	Gnd	Gnd	Gnd
21	TCP14_RSDS_A1P	1.25V	Open
22	TCP14_RSDS_A1N	1.18V	Open

Pin	Label	Run	Diode Check
23	TCP14_RSDS_A2P	1.25V	Open
24	TCP14_RSDS_A2N	1.18V	Open
25	TCP14_RSDS_A3P	1.25V	Open
26	TCP14_RSDS_A3N	1.18V	Open
27	Gnd	Gnd	Gnd
28	TCP13_RSDS_A1P	1.25V	Open
29	TCP13_RSDS_A1N	1.18V	Open
30	TCP13_RSDS_A2P	1.25V	Open
31	TCP13_RSDS_A2N	1.18V	Open
32	TCP13_RSDS_A3P	1.25V	Open
33	TCP13_RSDS_A3N	1.18V	Open
34	Gnd	Gnd	Gnd
35	RSDS_CLK_P9	1.08V	Open
36	RSDS_CLK_N9	1.34V	Open
37	Gnd	Gnd	Gnd
38	TCP12_RSDS_A1P	1.25V	Open
39	TCP12_RSDS_A1N	1.18V	Open
40	TCP12_RSDS_A2P	1.25V	Open
41	TCP12_RSDS_A2N	1.18V	Open
42	TCP12_RSDS_A3P	1.25V	Open
43	TCP12_RSDS_A3N	1.18V	Open
44	Gnd	Gnd	Gnd

Pin	Label	Run	Diode Check
45	RSDS_CLK_PB	1.08V	Open
46	RSDS_CLK_NB	1.34V	Open
47	Gnd	Gnd	Gnd
48	TCP11_RSDS_A1P	1.25V	Open
49	TCP11_RSDS_A1N	1.18V	Open
50	TCP11_RSDS_A2P	1.25V	Open
51	TCP11_RSDS_A2N	1.18V	Open
52	TCP11_RSDS_A3P	1.25V	Open
53	TCP11_RSDS_A3N	1.18V	Open
54	Gnd	Gnd	Gnd
55	n/c	n/c	Open
56	n/c	n/c	Open
57	3.3V	3.28V	Open
58	3.3V	3.28V	Open
59	3.3V	3.28V	Open
60	3.3V	3.28V	Open



57~60 pins
3.3V TP

White hash marks count as 5

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

MAIN BOARD SECTION

The following section gives detailed information about the Main board. This board contains the Microprocessor, Audio section, video section and all AV inputs. It also receives all input signals and processes them to be delivered to the Control board via the LVDS cable.
The (VSB, 8VSB and QAM) Silicon tuner is located on the Main board. The Main board is also where the television's software upgrades are accomplished through the USB port.

This board has no mechanical adjustments.

The Main Board Receives its operational voltage from the SMPS:

DURING STAND-BY FROM THE SMPS:

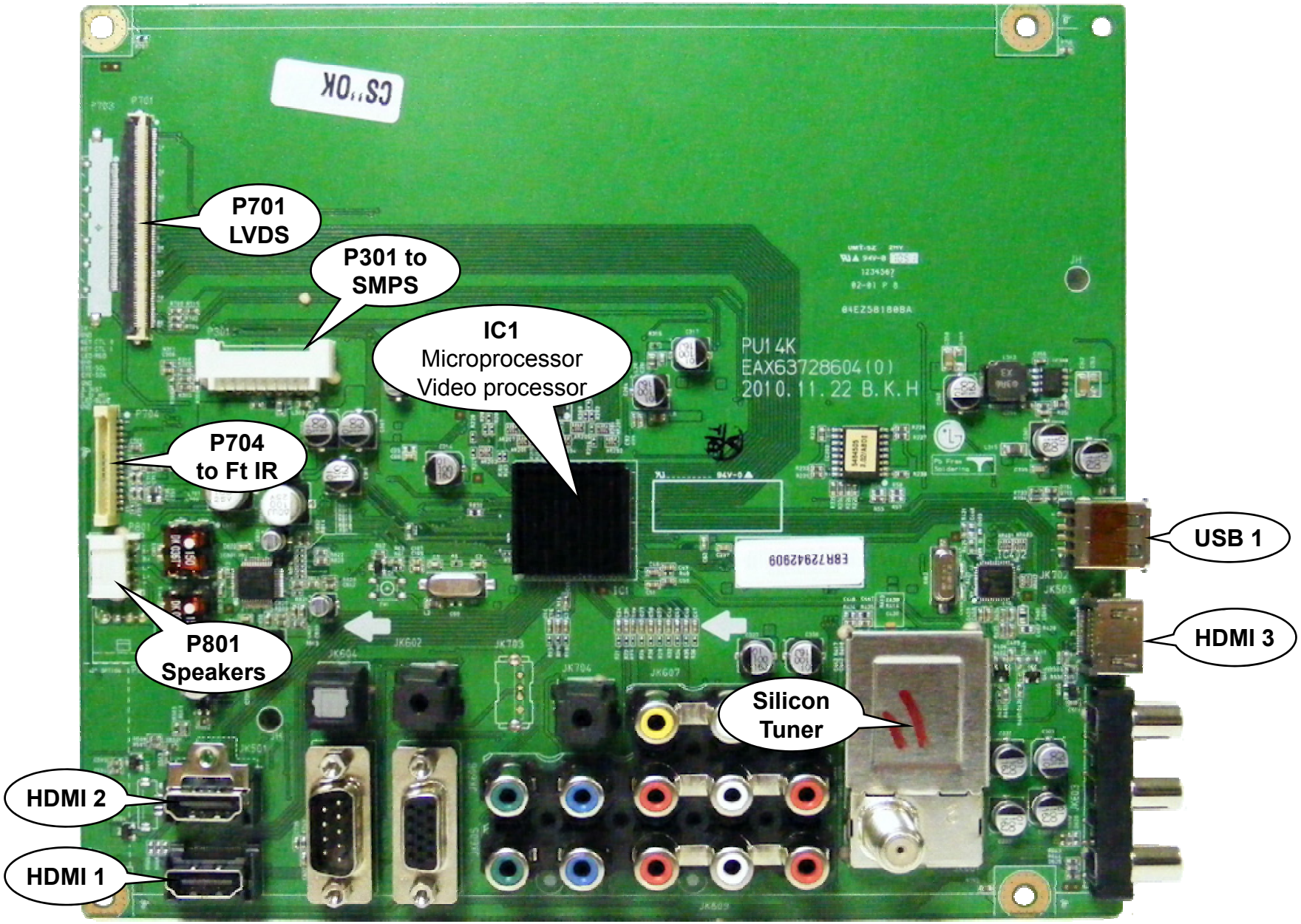
- **STBY 5V (3.4V in STBY and 5.1V during run).**

DURING RUN FROM THE SMPS (STBY 5V remains):

- **+5V for Video processing**
- **17V for Audio amplification**

- Distributes Key_CTL_0 and Key_CTL_1 to the Front IR Board for Front Key Pad detection.
- Receives Intelligent Sensor data from the Front IR/Key Board (via SCL/SDA).
- Drives front Power LEDs.
- Distributes +3.3V_ST and 5V_MST to the Front IR Board.

Main Board Layout and Identification



50PV450 Main (Front and Back) Layout Drawing

P301 "Main" to P813 "SMPS"

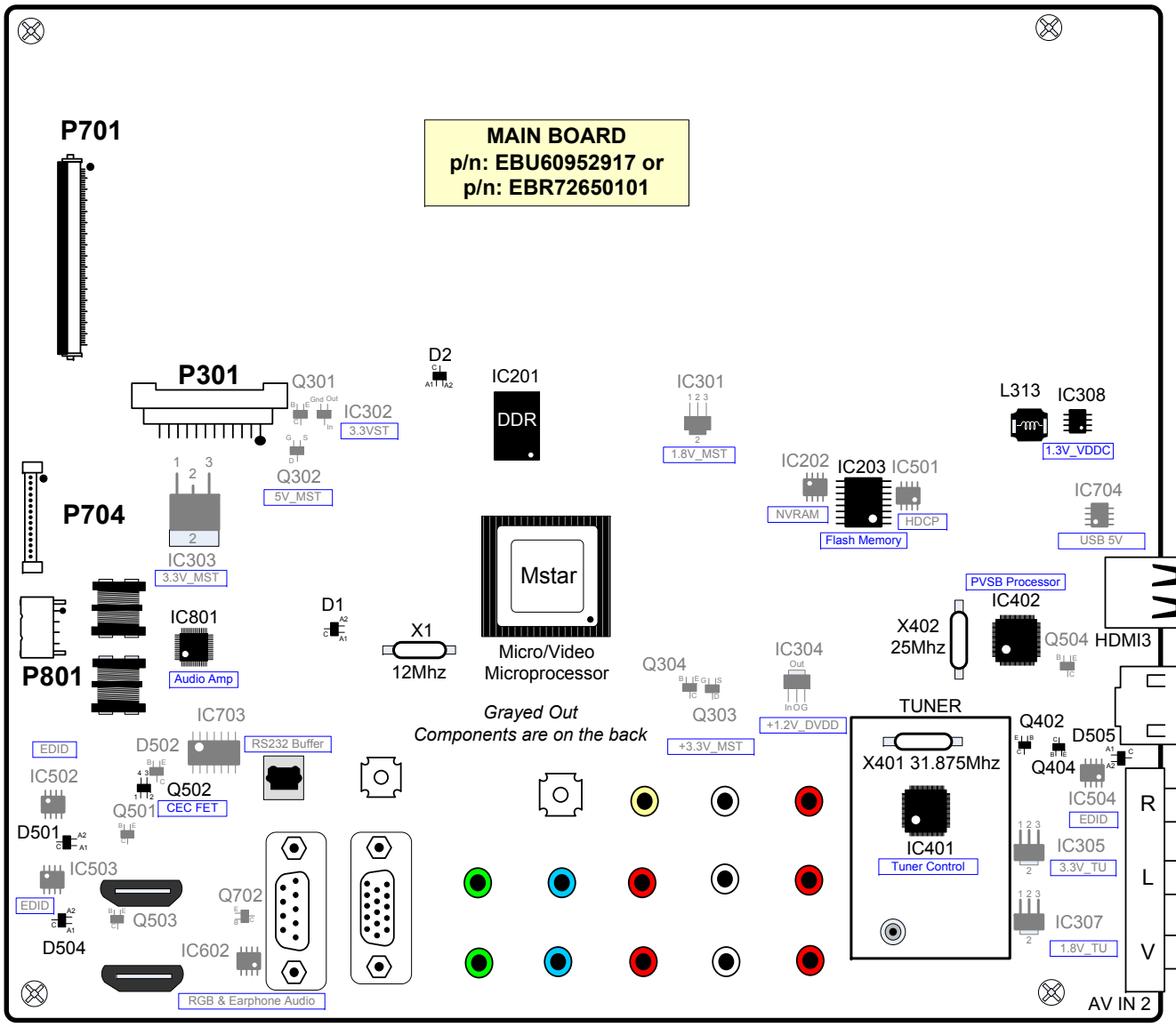
Pin	Label	Stby	Run	Diode
1-2	[a]17V	0V	17V	OL
3-4	Gnd	Gnd	Gnd	Gnd
5-7	[a]5.1V	0.46V	5.1V	0.88V
8	[a c]Error_Det	2.87V	4.9V	3.05V
9-12	Gnd	Gnd	Gnd	Gnd
13-14	Stby_5V	3.4V	5.1V	1.02V
15	[a]RL_ON	0V	2.4V	2.6V
16	[a d]AC_Det	0V	4.4V	2.92V
17	[b]M_On	0V	3.2V	OL
18	[e]Auto_Gnd	Gnd	Gnd	Gnd

P801 "Main" to "Speakers"

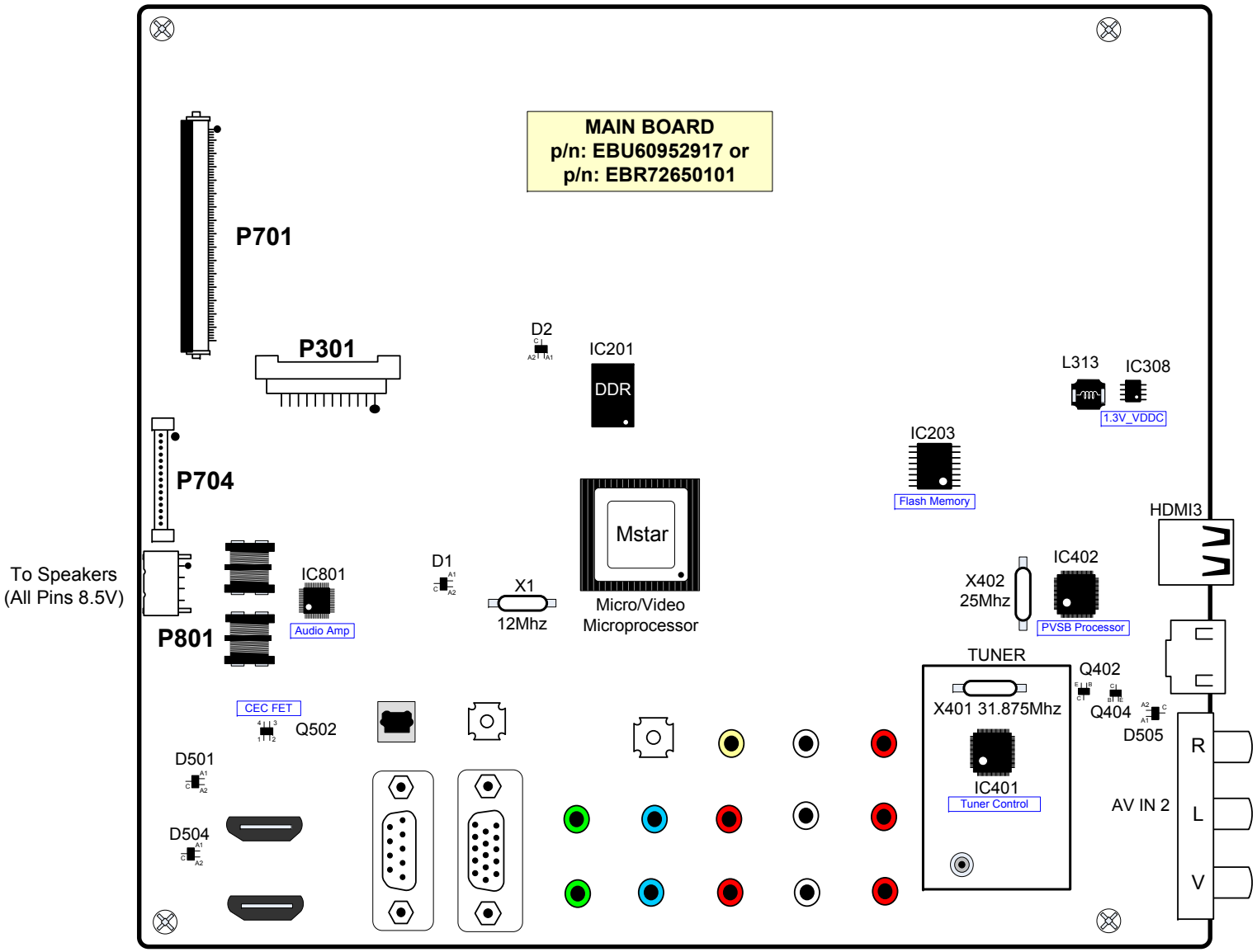
Pin	Label	SBY	Run	Diode
1	R-	0V	8.5V	Open
2	R+	0V	8.5V	Open
3	L-	0V	8.5V	Open
4	L+	0V	8.5V	Open

P704 "MAIN" to "Front IR"

Pin	Label	STBY	RUN	Diode Chk
1	IR	3.3V	3.9V	3.14V
2	Gnd	Gnd	Gnd	Gnd
3	Key_Ctl_0	3.3V	3.3V	1.18V
4	Key_Ctl_1	3.3V	3.3V	1.18V
5	LED_Red	2.7V	0V	OL
6	Gnd	Gnd	Gnd	Gnd
7	EYE_SCL	3.1V	3.1V	OL
8	EYE_SDA	3.1V	3.1V	OL
9	Gnd	Gnd	Gnd	Gnd
10	3.3_VST	3.3V	3.3V	1.3V
11	3.3_MST	0V	5V	1.24V
12	LED_Blue	0V	0V	1.02V
13	Touch_Ver_Check	0.19V	0.19V	1.75V
14	n/c	n/c	n/c	OL
15	n/c	n/c	n/c	OL



50PV450 Main Front Layout Drawing



50PV450 Main Board Front Side Component Voltages

IC203 inbond Serial

Pin	Flash	Pin	
[1]	3.3V	[9]	0V
[2]	3.3V	[10]	Gnd
[3]	n/c	[11]	n/c
[4]	n/c	[12]	n/c
[5]	n/c	[13]	n/c
[6]	n/c	[14]	n/c
[7]	0.08V	[15]	0.08V
[8]	3.3V	[16]	0.08V

IC308 +1.3V_VDDC

Pin	Regulator
[1]	0.8V*
[2]	0V
[3]	5V
[4]	6.1V
[5]	5V
[6]	1.3V
[7]	1.3V
[8]	4.5V

*Caused Video to Mute

Q402 Tuner CVBS

Pin	Buffer (Analog)
[B]	1.1V
[E]	1.7V
[C]	Gnd

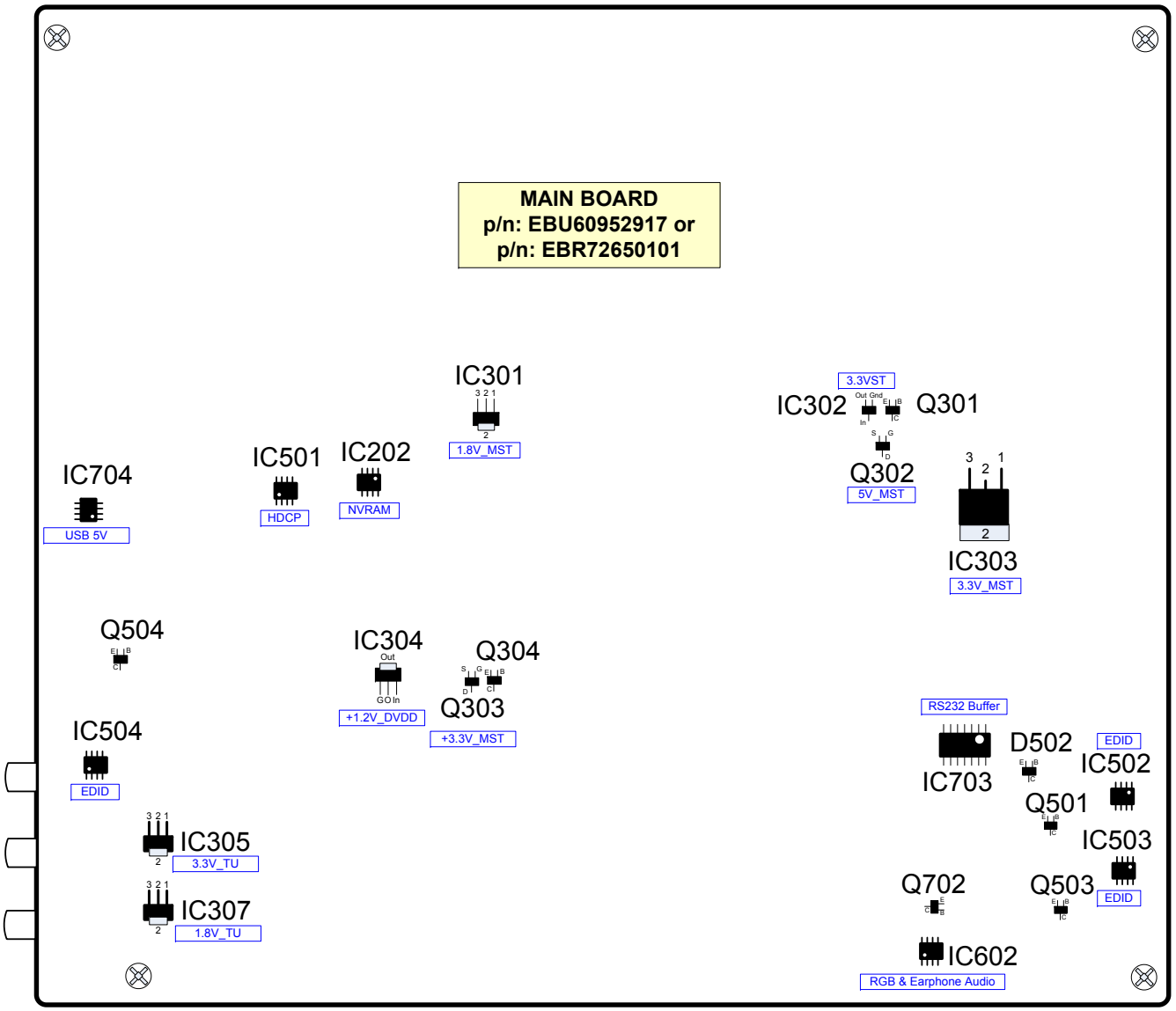
Q404 Tuner SIF

Pin	Buffer (Digital)
[B]	1.2V
[E]	1.8V
[C]	Gnd

Q502 HDMI CEC

Pin	Buffer
[1 B]	Gnd
[2 S]	3.18V
[3 D]	3.29V
[4 G]	3.3V

50PV450 Main Back Layout Drawing



50PV450 Main Board Back Side Component Voltages

IC202 **NVRAM**

Pin	
[1]	Gnd
[2]	Gnd
[3]	Gnd
[4]	Gnd
[5]	3.3V
[6]	3.3V
[7]	Gnd
[8]	3.3V

IC301 1.8V_MST

Pin	Regulator
[1]	0.6V
[2]	1.8V (Out)
[3]	3.3V (In)

IC302 3.3V_VST

Pin	Regulator
[1]	Gnd
[2]	3.3V (Out)
[3]	5.09V (In)

IC303 3.3V_MST

Pin	Regulator
[1]	Gnd
[2]	3.3V (Out)
[3]	5.04V (In)

IC304 1.2V_DVDD Reg

Pin	Dig Ch Only
[1]	Gnd
[2]	1.2V (Out)
[3]	3.3V (In)

IC305 3.3V_TU

Pin	Regulator
[1]	2.1V
[2]	3.3V (Out)
[3]	5.1V (In)

IC307 1.8V_TU

Pin	Regulator
[1]	Gnd
[2]	1.8V (Out)
[3]	3.3V (In)

IC501 HDCP Data

Pin	EEPROM
[1]	Gnd
[2]	Gnd
[3]	3.3V
[4]	Gnd
[5]	3.3V
[6]	3.3V
[7]	3.3V
[8]	3.3V

IC502 **IC503, IC504** EDID Data

Pin	For HDMI
[1]	Gnd
[2]	Gnd
[3]	Gnd
[4]	Gnd
[5]	3.3V
[6]	3.3V
[7]	3.3V
[8]	3.3V

IC602 RGB

Pin	Earphone Amp
[1]	Gnd
[2]	Gnd
[3]	Gnd
[4]	Gnd
[5]	5.09V
[6]	5.09V
[7]	0V
[8]	5.09V

Q303 3.3V_PVSB

Pin	Dig Ch Only
[G]	0V
[S]	3.3V
[D]	3.3V

Only on with Dig Channel

Q301 Driver for 5V_MST

Q302 5V_MST

Q304 urns on 3.3V_PVSB

IC703 RS232 Tx/Rx

Pin	
[1]	3.3V
[2]	5.6V
[3]	0V
[4]	0V
[5]	(-5.5V)
[6]	(-5.5V)
[7]	(-5.5V)
[8]	0V
[9]	3.3V
[10]	3.3V
[11]	n/c
[12]	n/c
[13]	0V
[14]	5.6V
[15]	Gnd
[16]	3.3V (B+)

IC704 USB 5V

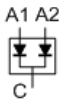
Pin	Limiter
[1]	Gnd
[2]	5.1V (In)
[3]	5.1V (In)
[4]	3.3V
[5]	0V
[6]	5.1V (Out)
[7]	5.1V (Out)
[8]	n/c

Q501, Q503
Q504 Hot Swap

Q702 RS232

Pin	Tx Buffer
[B]	0.6V
[C]	0V
[E]	Gnd

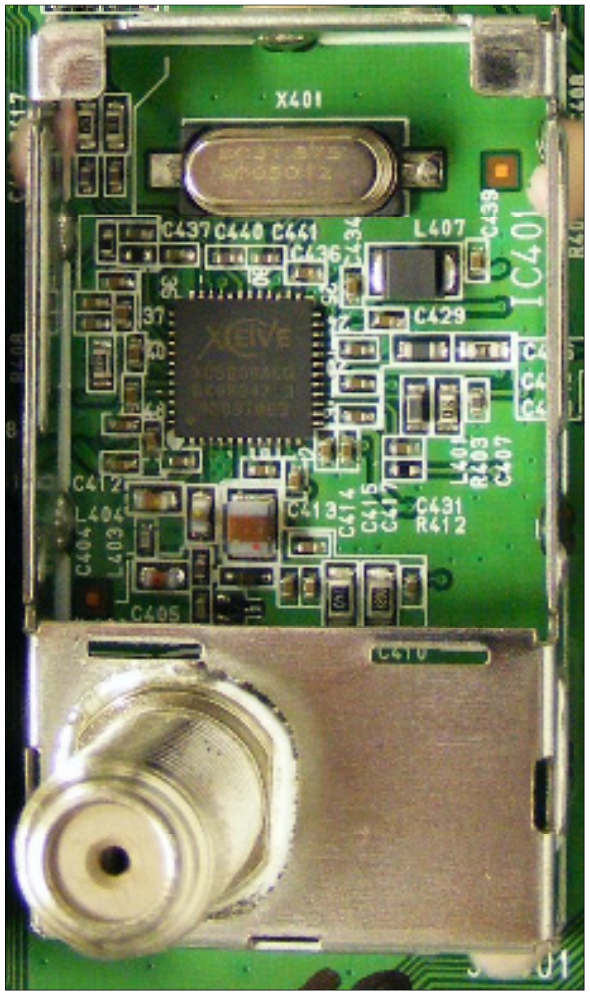
D502 HDMI CEC Limiter



Pin	
[A1]	0V
[A2]	3.28V
[C]	3.28V

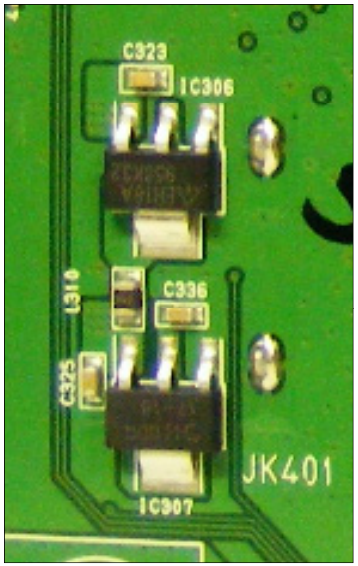
Main Board Tuner Explained

The Tuner in this set is discreet components (Silicon Tuner) and no longer a self contained unit (can).

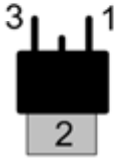


Front bottom right hand side

Check for Tuner B+:
3.3V on IC306 and 1.8V on IC307

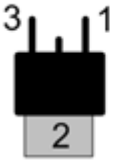


IC306 3.3V_TU



Pin Regulator
[1] Gnd
[2] 3.3V (Out)
[3] 4.97V (In)

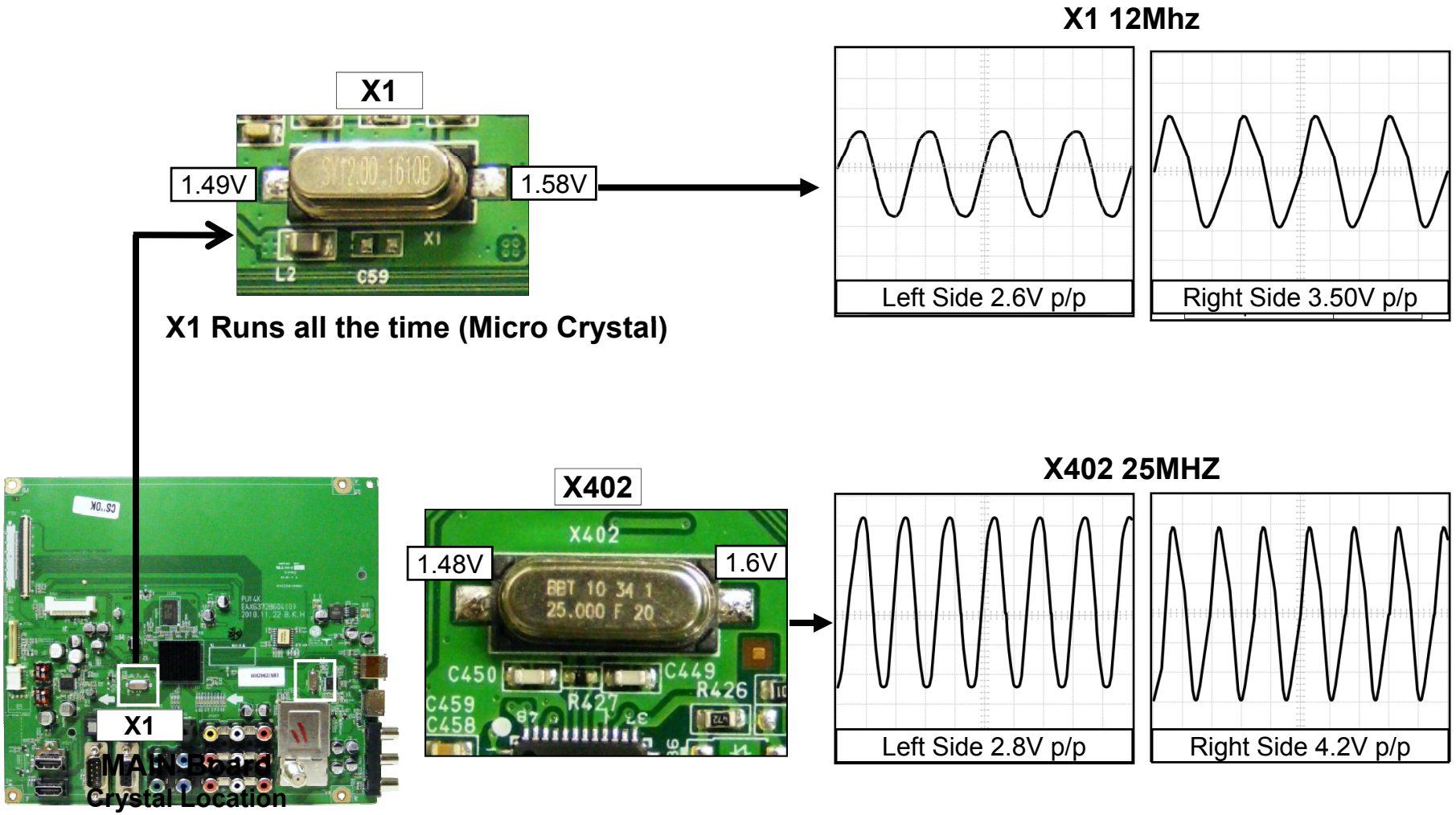
IC307 1.8V_TU



Pin Regulator
[1] Gnd
[2] 1.8V (Out)
[3] 3.3V (In)

Back Side bottom left hand side

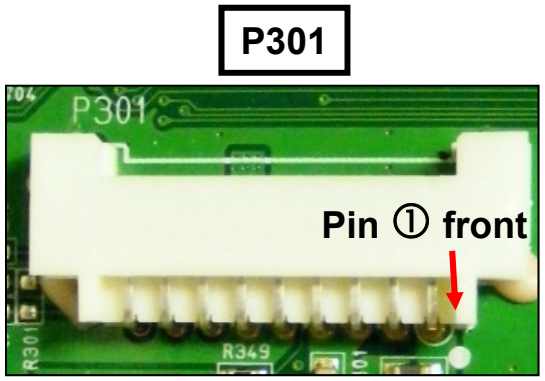
Main Board Crystal X1 and X402 Check



Main Board Plug P301 to Power Supply Voltages and Diode Check

P301 "Main" to P813 "SMPS"

Pin	Label	STBY	Run	Diode Check
1_2	[a]17V	0V	17V	OL
3-4	Gnd	Gnd	Gnd	Gnd
5-7	[a]5.1V	0.46V	5.1V	0.88V
8	[a] [c]Error_Det	2.87V	4.9V	3.05V
9-12	Gnd	Gnd	Gnd	Gnd
13-14	STBY_5V	3.4V	5.1V	1.02V
15	[a]RL_ON	0V	2.4V	2.6V
16	[a] [d]AC Det	0V	4.4V	2.92V
17	[b]M_ON	0V	3.2V	OL
18	[e]Auto_Gnd	Gnd	Gnd	Gnd



Front pins are odd
Back pins are even

[a] Note: The RL_On command turns on the 17V, +5V, Error_Det and AC_DET.
[b] Note: The M-On command turns on M5V, Va and Vs.
[c] Note: The Error Det line is not used in this model.
[d] Note: AC Det line if missing, the TV will attempt to turn on, but shut right back off.
[e] Note: Pin 18 is grounded on the Main. If opened, the power supply turns on automatically.

Diode Mode Check with the Board Disconnected. DVM in the Diode mode.

Main Board Plug P704 to Ft IR / Soft Touch Key Board

Voltage and Diode Mode Measurements for the Main Board

P704 "MAIN" to "Front IR"

Pin	Label	STBY	Run	Diode Check
1	IR	3.3V	3.9V	3.14V
2	Gnd	Gnd	Gnd	Gnd
3	Key_CTL_0	3.3V	3.3V	1.81V
4	Key_CTL_1	3.3V	3.3V	1.81V
5	LED_RED	2.7V	0V	OL
6	Gnd	Gnd	Gnd	Gnd
7	EYE_SCL	3.1V	3.1V	OL
8	EYE_SDA	3.1V	3.1V	OL
9	Gnd	Gnd	Gnd	Gnd
10	3.3VST	3.3V	3.3V	1.3V
11	3.3V_MST	0V	5V	1.24V
12	LED_BLUE	0V	0V	1.02V
13	Touch_Ver_Check	0.19V	0.19V	1.75V
14	n/c	n/c	n/c	OL
15	n/c	n/c	n/c	OL

Infrared Remote

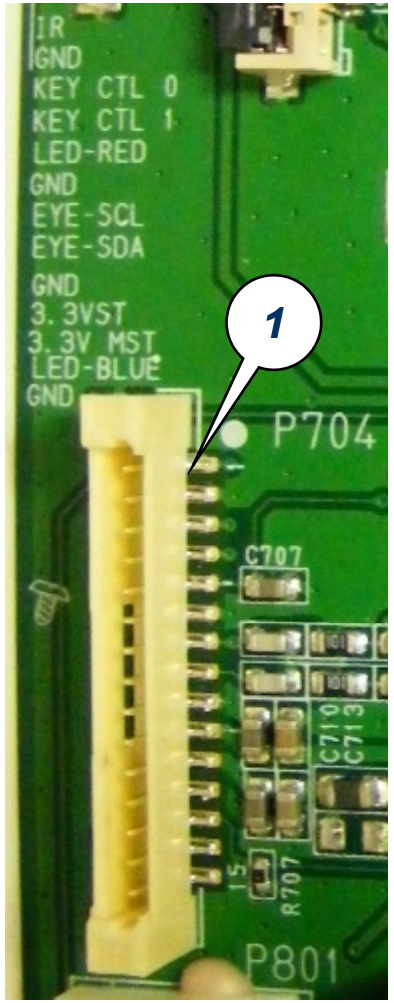
3 & 4 Function Buttons

7 & 8 Intelligent Sensor

Stand-By 3.3V

3.3V_Multi is actually +5V_MST

Soft Touch Key board sensitivity

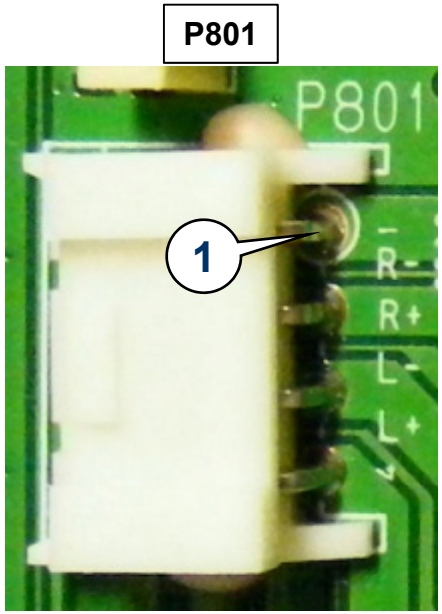


Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

Main Board P801 Connector Voltage and Diode Check

P801 "Main" to "Speakers"

Pin	Label	SBY	Run	Diode Check
1	R-	0V	8.5V	Open
2	R+	0V	8.5V	Open
3	L-	0V	8.5V	Open
4	L+	0V	8.5V	Open



Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

Main Board IC801 Audio Circuit Explanation

AUDIO OUT
Right – pin 39
Right + pin 36
Left - pin 1
Left + pin 46

AUDIO B+ 17V
Pins 2,3, 44, 45 (Left)
Pins 34, 35, 40, 41 (Right)

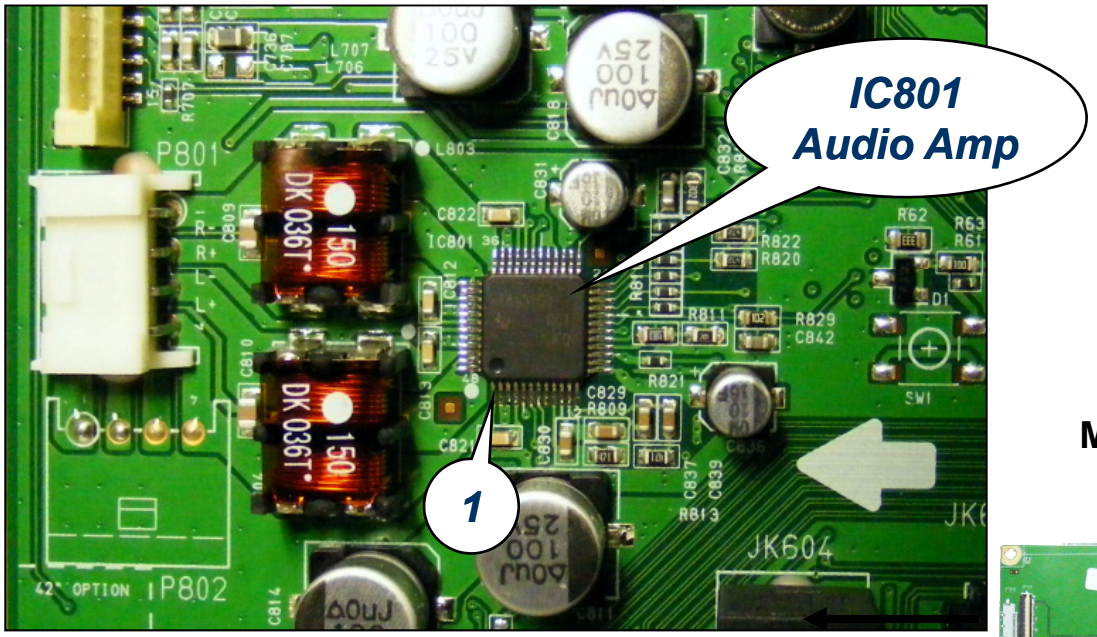
+3.3V_AMP_DVDD Arriving Pin 13, 27
From 3.3V_Normal through L1605
3.3V_Normal generated by IC505
Note: 3.3V_AMP_DVDD made by routing 3.3V_MST through a coil L801 or L802

All speaker pins 8.5V

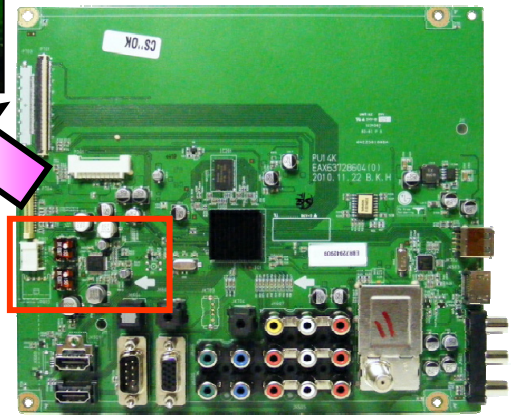
P801 Speaker Connector

Right (-)
Right (+)
Left (-)
Left (+)

See previous page For P801 Diode Check



Main Board Location



I2C Master Clk pin 15
AC_DET pin 19
LRCLK pin 20
TAS_RESET pin 25

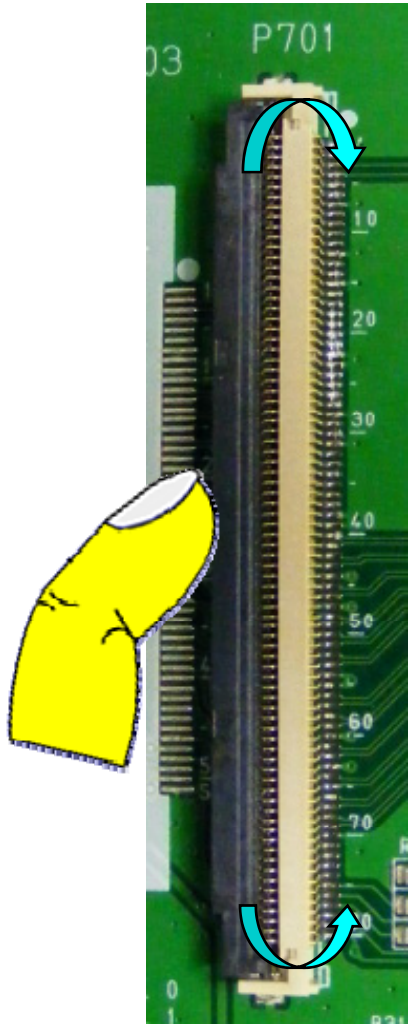
DATA pin 23
SCLK pin 24

Main Board P701 (Removing the LVDS Cable)

(1) Using your fingernail, lift up the locking mechanism.

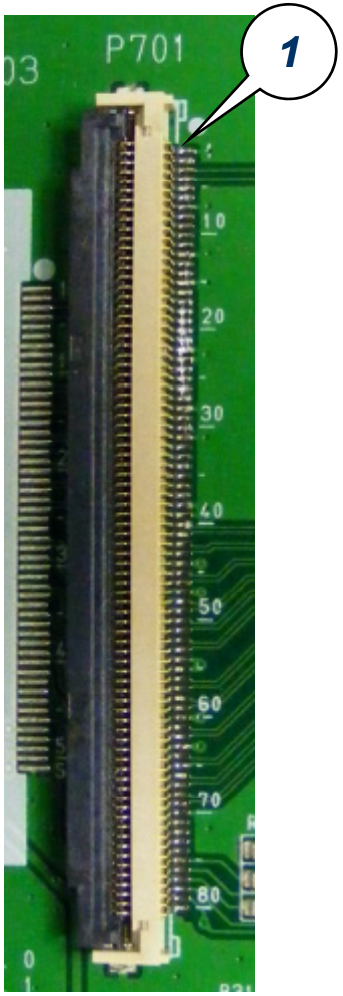
Since the locking tab is very thin and fragile, its best to lift slightly one end, then work across the locking tab a little at a time, back and forth until the tab is released.

(2) Pull the Cable from the Connector



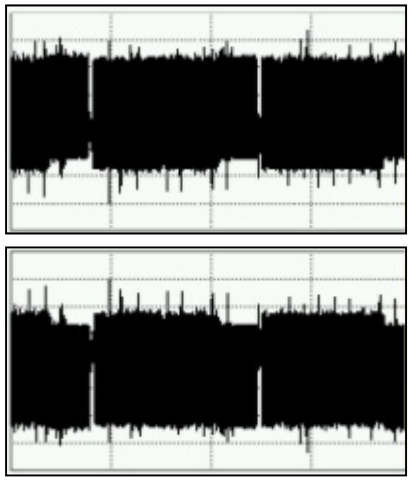
Main Board P701 LVDS Video Signal Checks

Pin Ctl Board	Pin Main Board	Pin Ctl Board	Pin Main Board
80	1	40	41
79	2	39	42
78	3	38	43
77	4	37	44
76	5	36	45
75	6	35	46
74	7	34	47
73	8	33	48
72	9	32	49
71	10	31	50
70	11	30	51
69	12	29	52
68	13	28	53
67	14	27	54
66	15	26	55
65	16	25	56
64	17	24	57
63	18	23	58
62	19	22	59
61	20	21	60
60	21	20	61
59	22	19	62
58	23	18	63
57	24	17	64
56	25	16	65
55	26	15	66
54	27	14	67
53	28	13	68
52	29	12	69
51	30	11	70
50	31	10	71
49	32	9	72
48	33	8	73
47	34	7	74
46	35	6	75
45	36	5	76
44	37	4	77
43	38	3	78
42	39	2	79
41	40	1	80



Example Waveforms Taken from P701 pins 68 and 68, but there are actually 20 pins carrying video, but they are all similar. Input Signal SMPT Color Bar

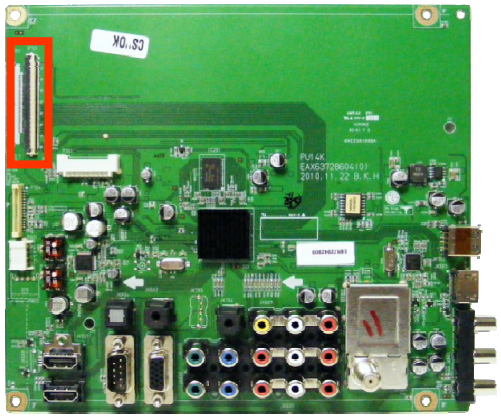
Pin 68	RE2-
Pin 69	RE2+



613mV p/p	10MSec per/div

TIP: Use the Control Board side for measurements. Test Points are available. Use the Pin cross reference chart on the left because the pins are inverted on the Control Board.

Main Board P701 Location



Main Board Plug P701 "LVDS" Voltages

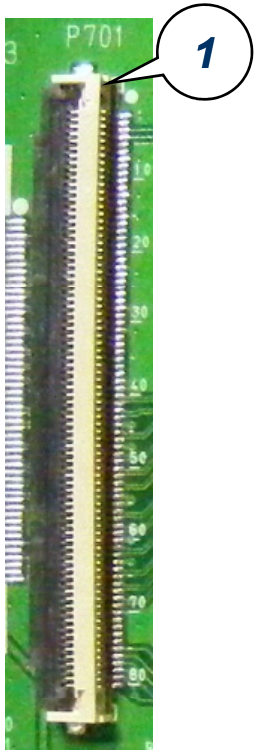
Voltage and Diode Test for the Main Board

P701 "Main LVDS" to P31 "Control" Note: For Voltage Measurements, use the Control Board.

Pin	Label	Run	Diode
1	Gnd	Gnd	Gnd
2	n/c	n/c	OL
3	ROM_RX	3.3V	1.17V
4	ROM_TX	3.3V	1.17V
5	n/c	n/c	OL
6	n/c	n/c	OL
7	Gnd	Gnd	Gnd
8	n/c	n/c	OL
9	n/c	n/c	OL
10	n/c	n/c	OL
11	n/c	n/c	OL
12	Gnd	Gnd	Gnd
13	n/c	n/c	OL
14	n/c	n/c	OL
15	Gnd	Gnd	Gnd
16	n/c	n/c	OL
17	n/c	n/c	OL
18	n/c	n/c	OL
19	n/c	n/c	OL
20	n/c	n/c	OL
21	n/c	n/c	OL
22	Gnd	Gnd	Gnd
23	Gnd	Gnd	Gnd
24	n/c	n/c	OL
25	n/c	n/c	OL
26	n/c	n/c	OL

Pin	Label	Run	Diode
27	n/c	n/c	OL
28	Gnd	Gnd	Gnd
29	n/c	n/c	OL
30	n/c	n/c	OL
31	Gnd	Gnd	Gnd
32	n/c	n/c	OL
33	n/c	n/c	OL
34	n/c	n/c	OL
35	n/c	n/c	OL
36	n/c	n/c	OL
37	n/c	n/c	OL
38	Gnd	Gnd	Gnd
39	Gnd	Gnd	Gnd
40	RA1-	1.11V	0.73V
41	RA1+	1.3V	0.73V
42	RB1-	1.11V	0.73V
43	RB1+	1.3V	0.73V
44	Gnd	Gnd	Gnd
45	RC1-	1.11V	0.73V
46	RC1+	1.3V	0.73V
47	Gnd	Gnd	Gnd
48	RCLK1-	1.2V	0.73V
49	RCLK1-	1.2V	1.04V
50	RD1-	1.11V	0.73V
51	RD1+	1.3V	0.73V
52	RE1-	1.11V	0.73V
53	RE1+	1.3V	0.73V

Pin	Label	Run	Diode
54	Gnd	Gnd	Gnd
55	Gnd	Gnd	Gnd
56	RA2-	1.11V	0.73V
57	RA2+	1.3V	0.73V
58	RB2-	1.11V	0.73V
59	RB2+	1.3V	0.73V
60	Gnd	Gnd	Gnd
61	RC2-	1.11V	0.73V
62	RC2+	1.3V	0.73V
63	Gnd	Gnd	Gnd
64	RCLK2-	1.2V	0.73V
65	RCLK2-	1.2V	1.04V
66	RD2-	1.11V	0.73V
67	RD2+	1.3V	0.73V
68	RE2-	1.11V	0.73V
69	RE2+	1.3V	0.73V
70	Gnd	Gnd	Gnd
71	n/c	n/c	n/c
72	n/c	n/c	n/c
73	n/c	n/c	n/c
74	n/c	n/c	n/c
75	Module_SDA1	3.3V	2.6V
76	DISP_EN	2.8V	0.48V
77	Module_SCL1	3.3V	2.6V
78	PC_SER_DATA	3.3V	1.44V
79	PC_SER_CLK	0.5V	0.98V
80	Gnd	Gnd	Gnd



Bold Indicates video signal

Note:
No Stand-By voltages.

Note:
Use the Control Board for Voltage Measurements.
See Pin cross reference table on preceding page.

Diode Mode Readings taken with all connectors Disconnected. DVM in Diode Mode.

FRONT IR / SOFT TOUCH KEY BOARD SECTION

The following section gives detailed information about the Front IR and Soft Touch Key board (IR/STKB). Note: The IR/STKB is attached to the Televisions Front Frame. It requires a great deal of disassembly to reach. After removing the bottom metal shield plate, the panel screws must be removed to lift up the panel in order to see the board. (Removing the panel allows better access).

The IR/STKB board contains the Infrared Remote Receiver, Intelligent Sensor and Soft Touch Key Board decoder. This board has no adjustments.

The IR/STKB receives its operational B+ from the Main Board:

- **3.3V_ST from the Main Board. This voltage is generated on the Power Supply. It is output on P704 pin 10. It arrives on the IR/STKB at P100 pin 10.**
- **3.3V_MST Generated on the Main Board by IC303 and output on P704 pin 11. It arrives on the IR/STKB at P100 pin 11.**

The IR signal is routed back to the Main Board via pin 1.

The Intelligent sensor is driven by 2 separate pins from the Main board SCL/SDA P100 pins 7 and 8. This sensor monitors the average room light and configures this information in data form back to the Microprocessor to manipulate brightness and color settings to correspond to room lighting conditions.

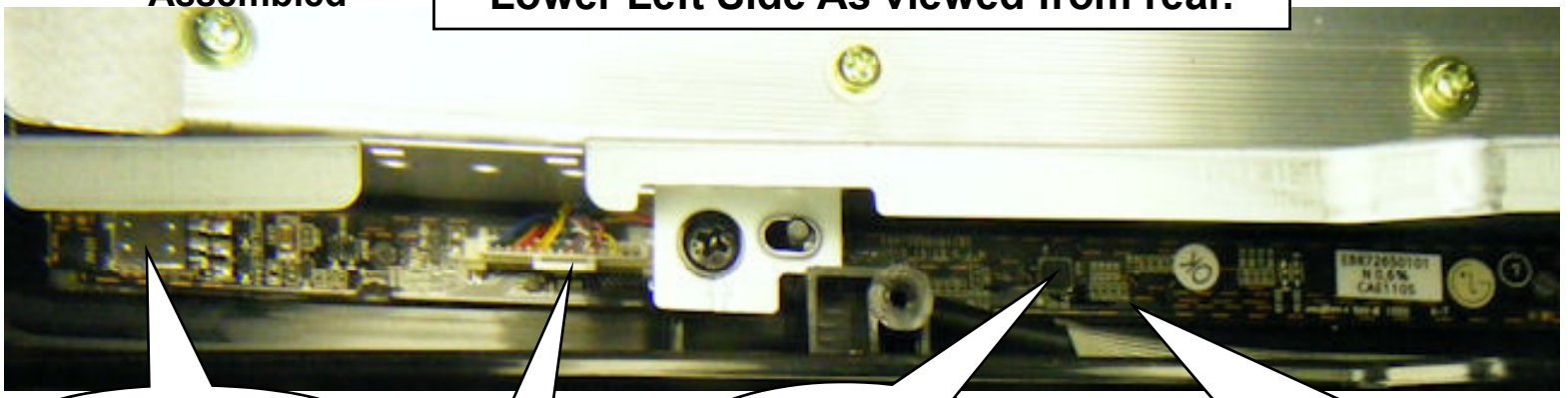
Pin 13 is Touch Version Check pin to adjust the sensitivity of the Soft Touch Keys.

The IR/STKB also has the Power LEDs. The control for the Power LEDs is routed in P100 pins 5 (LED_RED) and 12 (LED_BLUE).

IR / Soft Touch Key board and Intelligent Sensor Location

Assembled

Lower Left Side As viewed from rear.



IR Receiver

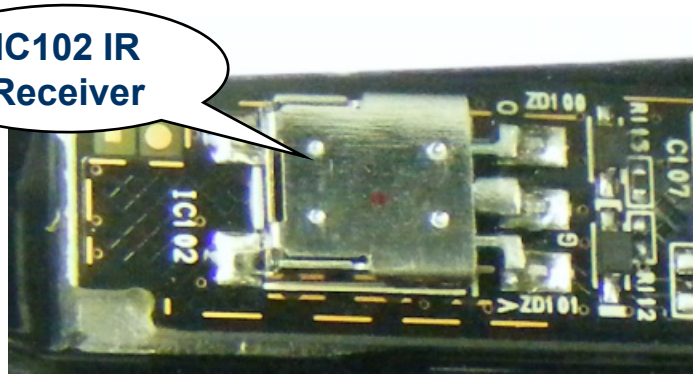
P100 To Main

Key Pad Decoder

Soft Touch Key Pad is part of the circuit board.

Note: The IR/STKB is attached to the Televisions Front Frame. It requires a great deal of disassembly to reach. After removing the bottom metal shield plate, the panel screws must be removed to lift up the panel in order to see the board.

IC102 IR Receiver



IC102 IR Receiver

O	Label	Readings
G	V: B+	0V
	O: Output	3.24V
V	G: Ground	2.85V

P901 (IR / STKB and Intelligent Sensor) Voltages and Pin Identification

P901 Connector "MAIN Board" To "IR Board"

Pin	Label	STBY	Run	Diode Check
1	SCL	2.9V	3.49V	3.28V
2	SDA	2.92V	3.49V	3.28V
3	Gnd	Gnd	Gnd	Gnd
4	KEY 1	3.26V	3.28V	1.88V
5	KEY 2	3.26V	3.28V	1.88V
6	3.5V_ST	3.55V	3.49V	1.15V
7	Gnd	Gnd	Gnd	Gnd
8	LED_B/BUZZ	0V	0V	OL
9	IR	1.48V	1.45V	OL
10	Gnd	Gnd	Gnd	Gnd
11	+3.3V_Normal	0.35V	3.34V	0.53V
12	LED_R/BUZZ	0V	0V	2.67V
13	Gnd	Gnd	Gnd	Gnd
14	S/T_SCL	3.55V	3.49V	1.86V
15	S/T_SDA	3.55V	3.49V	1.86V

Diode Mode Readings taken with all connectors Disconnected. Black lead on Gnd. DVM in Diode Mode.

Soft Touch Key Pad Voltage Checks

IC100 on the Front IR, Soft Touch Keys, Intelligent Sensor Board is generating these Resistance changes when a Soft Touch Key is touched. This in turn pulls down the Key 1 and Key 2 lines to be interpreted by the Microprocessor.

P1 Voltage Measurements with Soft Touch Key pressed.

Key 1 Line

KEY 1	Pin 3 measured from Gnd
Power	2.4V
CH (Up)	0.21V
CH (Dn)	1.6V
Input	0.88V

Key 2 Line

KEY 2	Pin 4 measured from Gnd
Enter	2.4V
Volume (-)	0.21V
Menu	1.6V
Volume (+)	0.88V

P900 "Main" (No Key Pressed)

Pin	Label	STBY	Run
3	KEY 1	3.26V	3.28V
4	KEY 2	3.26V	3.28V

INVISIBLE SPEAKER SYSTEM SECTION

Invisible Speaker System Overview (Full Range Speakers)

p/n: EAB62028901

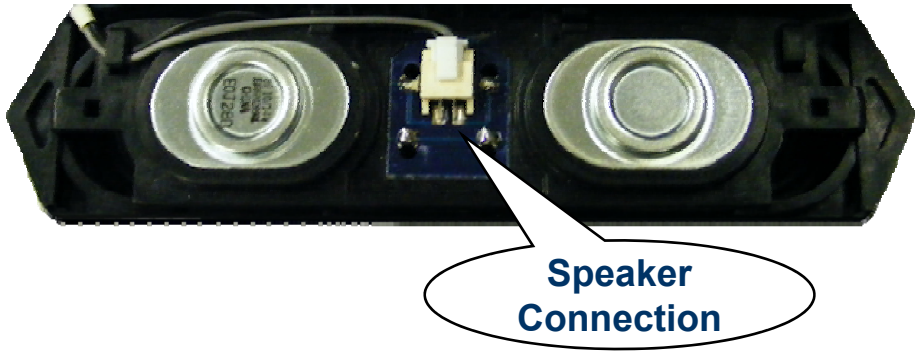
The 50PV450 contains the Invisible Speaker system.
The Full Range Speakers point downward, so there are no front viewable speaker grills or air ports.

Installed Bottom View

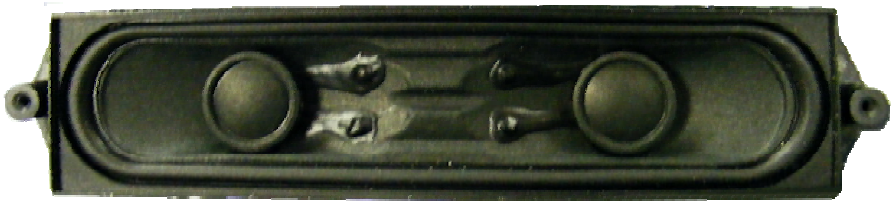
Remove two screws from the bottom

Reading across speaker wires, 8.2 ohm.

Rear View



Front View

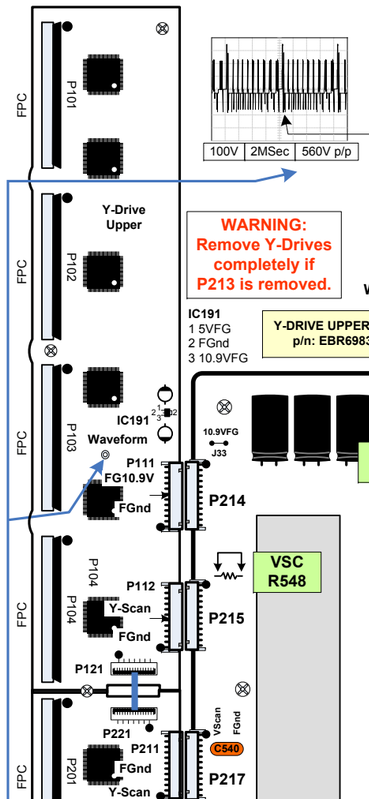


This section shows the Interconnect Diagram called the 11X17 foldout that's available in the Paper and Adobe version of the Training Manual.

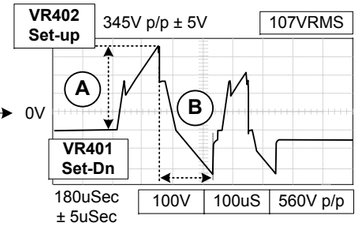
Use the Adobe version to zoom in for easier reading.

When Printing the Interconnect diagram, print from the Adobe version and print onto 11X17 size paper for best results.

50PV450 (50R3 Panel) CIRCUIT INTERCONNECT DIAGRAM



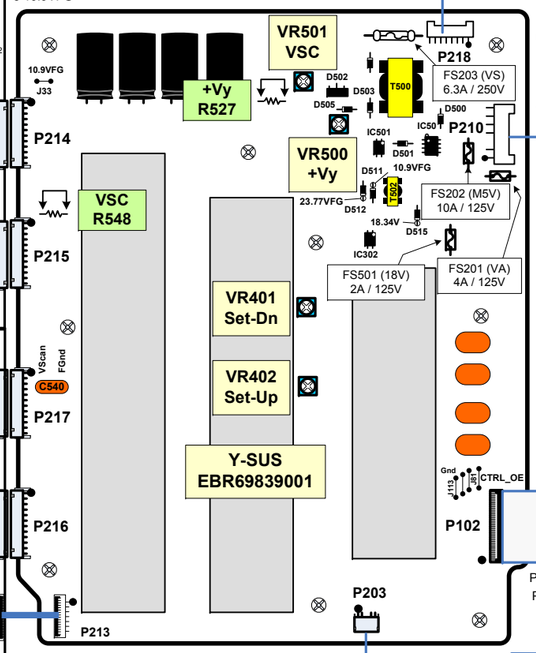
WARNING: Remove Y-Drives completely if P213 is removed.



Connect Scope between Waveform TP on Y-Drive and Gnd

IC191
1 5VFG
2 FGnd
3 10.9VFG

Y-DRIVE UPPER BOARD p/n: EBR69839101



FS201 Va or FS203 Vs Diode Check reads Open with Board Disconnected or Connected

FS202 M5V Diode Check reads 0.73V Board Connected or 1.38V Disconnected

FS501 18V Diode Check reads 1.28V Board Connected or 1.31V Disconnected

SMPS Test – Unplug P813 to Main board.
Use two (100W) light bulbs in series between Vs and Gnd to place a load on the SMPS. Apply AC, all voltage should run.
See "Auto Gen" on the Control board to perform a Panel Test.
If all supplies do not run when A/C is applied, disconnect P811 to isolate the excessive load.

With the unit on, if D1 is not on, check 5V supply. If present replace the Control Board.
If missing, see (To Test Power Supply)

CTRL_OE should be 0V
(5V indicates a Problem)

P811 "Power Supply" to P210 "Y-SUS"

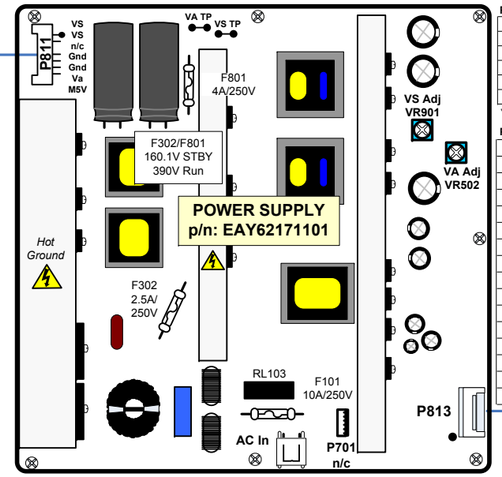
Pin	Label	Run	Diode
1~2	Vs	*201V	Open
3	n/c	n/c	n/c
4~5	Gnd	Gnd	Gnd
6	Va	*55V	Open
7	M5V	5.0V	1.38V

*Voltage varies with panel label

P813 "SMPS" to P301 "Main"

Pin	Label	Stby	Run	Diode
1-2	[a]17V	0V	17V	3.06V
3-4	Gnd	Gnd	Gnd	Gnd
5-7	[a]5.1V	0.46V	5.1V	2.13V
8	[a c]Error_Det	2.87V	4.9V	2.84V
9-12	Gnd	Gnd	Gnd	Gnd
13-14	Stby_5V	3.4V	5.1V	2.53V
15	[a]RL_ON	0V	2.4V	OL
16	[a d]AC_Det	0V	4.4V	3.1V
17	[b]M_On	0V	3.2V	OL
18	[e]Auto_Gnd	Gnd	Gnd	OL

Note a: The RL_On command turns on the 17V, +5V, Error_Det and AC_DET.
Note b: The M-On command turns on M5V, Va and Vs.
Note c: The Error Det line is not used in this model.
Note d: AC Det if missing TV will attempt to turn on but shuts back off.
Note e: Pin 18 is grounded on the Main. If opened, the power supply turn on automatically.



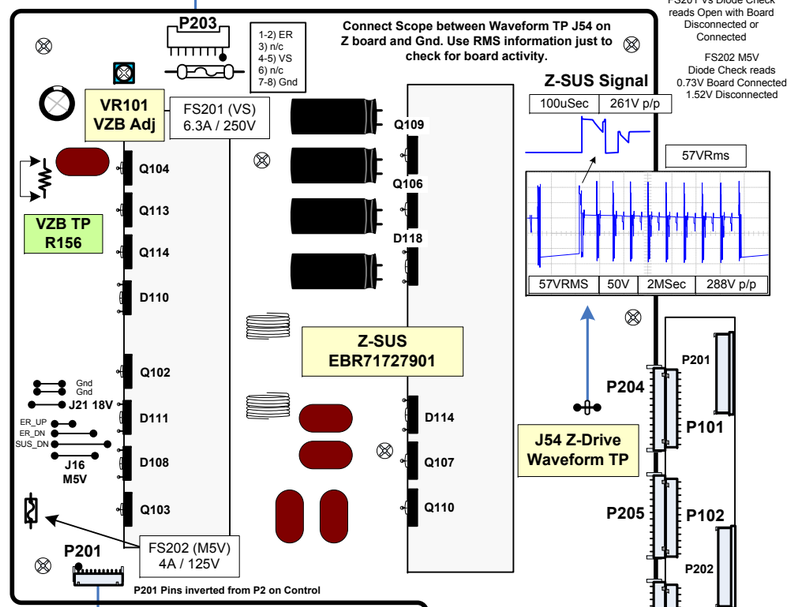
P203 "Z-SUS" to "Y-SUS" P218

Pin	Label	Run	Diode
1~2	ER_PASS	98V~102V	Open
3	n/c	n/c	n/c
4~5	+Vs	*201V	Open
6	n/c	n/c	n/c
7~18	Gnd	Gnd	Gnd

*Voltage varies with panel label

P2 "Control" to "Z-SUS Board" P201

Pin	Label	Run	Diode
15	(+15V)	18.34V	Open
14	(+15V)	18.34V	Open
13	n/c	n/c	1.52V
12	M5V	4.89V	1.52V
11	M5V	4.89V	1.52V
10	Gnd	Gnd	Gnd
9	Gnd	Gnd	Gnd
8	SUS_DN	0.73V	Open
7	CTRL_EN	0.06V	Open
6	SUS_UP	0.15V	Open
5	VZB2	2.49V	Open
4	ER_DN	0.1V	Open
3	VZB1	2.53V	Open
2	ER_UP	0.87V	Open
1	ZBIAS	1.9V	Open



FS201 Vs Diode Check reads Open with Board Disconnected or Connected

FS202 M5V Diode Check reads 0.73V Board Connected 1.52V Disconnected

To run Z-SUS stand-alone, jump 5V to Fuse FS202. Jump Audio B+ from SMPS to J21 on the Z-SUS. Disconnect Y-SUS from Control board and from the Z-SUS. Jump VS from SMPS to Z-SUS P203. J54 290V p/p (More square shape).

P801 "Main" to "Speakers"

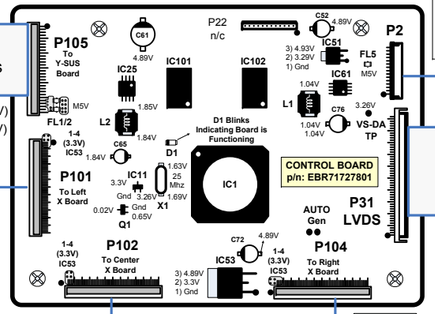
Pin	Label	SBY	Run	Diode
1	R-	0V	8.5V	Open
2	R+	0V	8.5V	Open
3	L-	0V	8.5V	Open
4	L+	0V	8.5V	Open

M5V Gnd Gnd M5V
FL1, FL2, FL5

18V To Z-SUS (In P105 pins 14-15) (Out P2 pins 14-15) Diode Check All Connectors Connected 1.28V

Ribbon Cable
Y-SUS and Y Drive Signals

Pins 6-8 (18V) Pins 3-5 (5V)
Pins 23-25 (18V) Pins 26-28 (5V)



Ribbon Cable
LVDS
See 2nd page for Waveforms

P213 "Y-SUS" to "Lower "Y-Drive" P213

Pin	Label	Run	Diode Check
1	M5V	4.96V	1.38V
2	M5V	4.96V	1.38V
3	OC2_B	2.77V	Open
4	Gnd	Gnd	Gnd
5	DATA_B	0V	1.85V
6	Gnd	Gnd	Gnd
7	OC1_B	1.73V	1.85V
8	OC2_T	2.73V	Open
9	Gnd	Gnd	Gnd
10	DATA_T	0V	1.85V
11	Gnd	Gnd	Gnd
12	OC1_T	1.74V	1.85V
13	Gnd	Gnd	Gnd
14	CLK	0.68V	1.85V
15	STB	4.27V	1.85V

Black Lead on Chassis Gnd

Y-DRIVE LOWER BOARD p/n: EBR69839201

P214 "Y-SUS" to "Upper Y-Drive" P111

Pin	Label	Run
1-2	FG10.9V	4.89V
3-12	FGnd	FGnd

Black Lead on Floating Gnd

P215 "Y-SUS" to "Upper Y-Drive" P112

Pin	Label	Run
1-7	FGnd	FGnd
8	n/c	n/c
9-12	Vscan	107V

Black Lead on Floating Gnd

P217 "Y-SUS" to "Lower Y-Drive" P211

Pin	Label	Run
1-4	Vscan	107V
5	n/c	n/c
6-12	FGnd	FGnd

Black Lead on Floating Gnd

P216 "Y-SUS" to "Lower Y-Drive" P212

Pin	Label	Run
1-10	FGnd	FGnd
11-12	Vscan	107V

Black Lead on Floating Gnd

Use left side of C540 to measure Y-Drive signal without Y-Drive.
454V p/p with Y-Drives
386V p/p without Y-Drives

P203 "Y-SUS" to "X-Drive Left" P121

Pin	Run	Diode Check
1-2	Gnd	Gnd
3	nc	nc
*4-5	VA Voltage	Open

*Voltage varies with panel label

To Test Control board:
Disconnect all connectors.
Jump STBY 5V from SMPS P813 Pin 13.
Apply AC and turn on the Set. Observe Control board LED, if it's on, most likely Control board is OK.

Note: IC53 (3.3V Regulator) routed to all X Boards

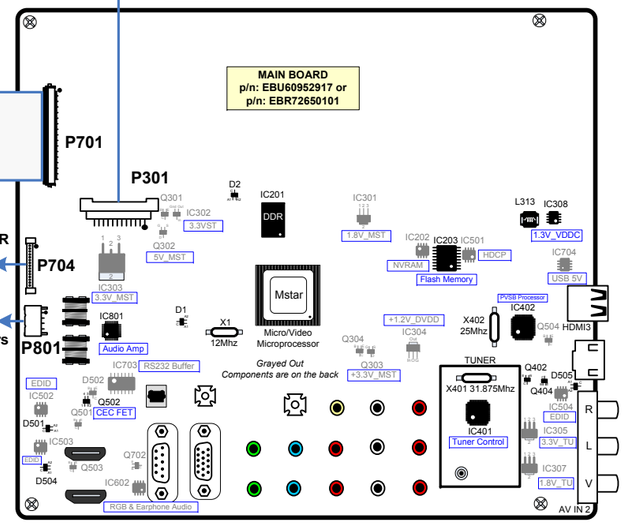
* If the complaint is no video and shorting the points (AutoGen) causes video to appear suspect the Main board or LVDS cable.
Note: LVDS Cable must be removed for Auto Gen to work.

PANEL TEST:
Remove LVDS Cable. Short across Auto Gen TPs to generate a test pattern.

P704 "MAIN" to "Front IR"

Pin	Label	STBY	RUN	Diode Chk
1	IR	3.3V	3.9V	3.14V
2	Gnd	Gnd	Gnd	Gnd
3	Key_Ctl_0	3.3V	3.3V	1.18V
4	Key_Ctl_1	3.3V	3.3V	1.18V
5	LED_Red	2.7V	0V	OL
6	Gnd	Gnd	Gnd	Gnd
7	EYE_SCL	3.1V	3.1V	OL
8	EYE_SDA	3.1V	3.1V	OL
9	Gnd	Gnd	Gnd	Gnd
10	3.3_VST	3.3V	3.3V	1.3V
11	3.3_MST	0V	5V	1.24V
12	LED_Blue	0V	0V	1.02V
13	Touch_Ver_Check	0.19V	0.19V	1.75V
14	n/c	n/c	n/c	OL
15	n/c	n/c	n/c	OL

To Ft IR (A)
To Speakers



P100
To P704 Main (A)
Ft IR/Key Pad

Attached to front glass

IR/Key Board p/n: EBR72650101

Diode Check
Va: Open Blk on Gnd.

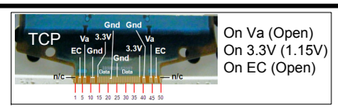
P121 "X Left" to P203 "Y-SUS"

Pin	Run	Diode Check
1,2	VA Voltage	Open
3	nc	nc
4,5	Gnd	Gnd

X-Board Left p/n: EBR71728101
P121 P201 P202 P203 P204 P205
P110 3.3V in on Pins 57~60
P120 Va out on Pins 1~2

X-Board Center p/n: EBR71728401
P320 Va in on Pins 1~2
P310 3.3V in on Pins 57~60
P321 Va out on Pins 1~2
P201 P202 P203 P204 P205

X-Board Right p/n: EBR71728501
P320 Va in on Pins 1~2
P310 3.3V in on Pins 57~60



On Va (Open)
On 3.3V (1.15V)
On EC (Open)

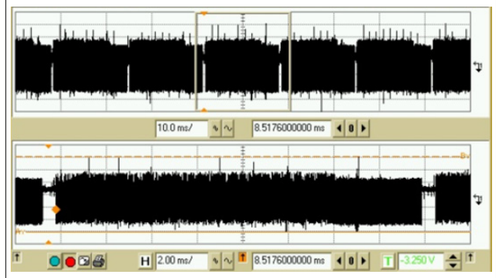
P201 P202 P203 P204 P205

50PV450 LVDS P31 Control Board from P701 Main Board Waveform Samples

P31 Control	P701 Main	
80	1	
79	2	
78	3	RXD
77	4	TXD
76	5	
75	6	
74	7	
73	8	
72	9	
71	10	
70	11	
69	12	
68	13	
67	14	
66	15	
65	16	
64	17	
63	18	
62	19	
61	20	
60	21	
59	22	
58	23	
57	24	
56	25	
55	26	
54	27	
53	28	
52	29	
51	30	
50	31	
49	32	
48	33	
47	34	
46	35	
45	36	
44	37	
43	38	
42	39	
41	**40**	Video
40	**41**	Video
39	**42**	Video
38	**43**	Video
37	44	
36	45	CLK
35	46	CLK
34	47	
33	**48**	Video
32	**49**	Video
31	**50**	Video
30	**51**	Video
29	**52**	Video
28	**53**	Video
27	54	
26	55	
25	**56**	Video
24	**57**	Video
23	**58**	Video
22	**59**	Video
21	60	CLK
20	61	CLK
19	62	
18	63	
17	**64**	Video
16	**65**	Video
15	**66**	Video
14	**67**	Video
13	**68**	Video
12	**69**	Video
11	70	
10	71	
9	72	
8	73	
7	74	
6	75	
5	76	Disp_En
4	77	
3	78	
2	79	
1	80	

RA1_- Video Signal

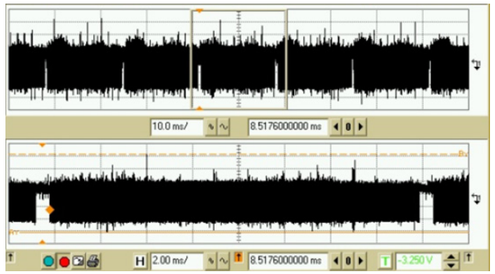
P31 LVDS (Pin 12) 10Msec / 613mV
Note: Pin 13 is Same but Inverted



Bottom Waveform at 2uSec

RB1_- Video Signal

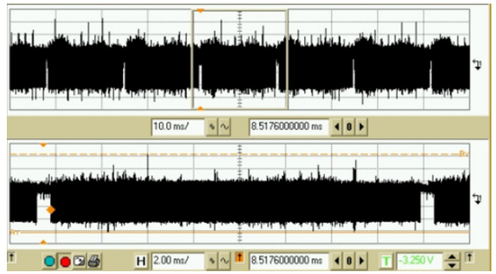
P31 LVDS (Pin 14) 10Msec / 627.5mV
Note: Pin 15 is Same but Inverted



Bottom Waveform at 2uSec

RC1_- Video Signal

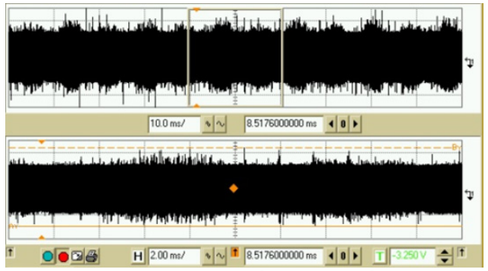
P31 LVDS (Pin 16) 10Msec / 638mV
Note: Pin 17 is Same but Inverted



Bottom Waveform at 2uSec

CLK1_- Clock Signal

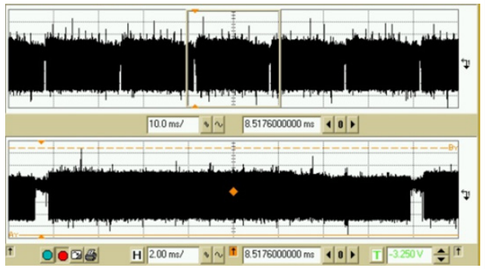
P31 LVDS (Pin 19) 10Msec / 638mV
Note: Pin 20 is Same but Inverted



Bottom Waveform at 2uSec

RD1_- Video Signal

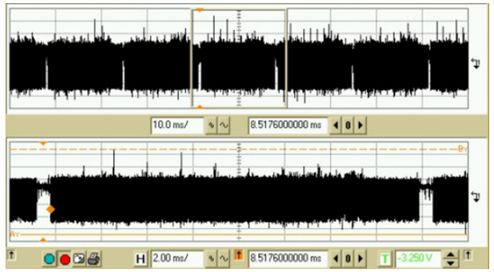
P31 LVDS (Pin 22) 10Msec / 714.6mV
Note: Pin 23 is Same but Inverted



Bottom Waveform at 2uSec

RE1_- Video Signal

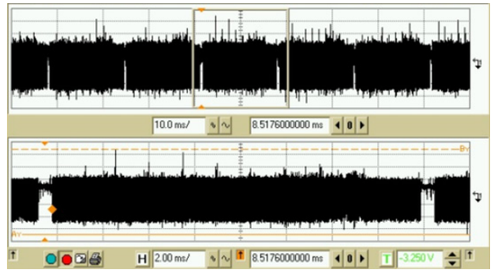
P31 LVDS (Pin 24) 10Msec / 686.7mV
Note: Pin 25 is Same but Inverted



Bottom Waveform at 2uSec

RA2_- Video Signal

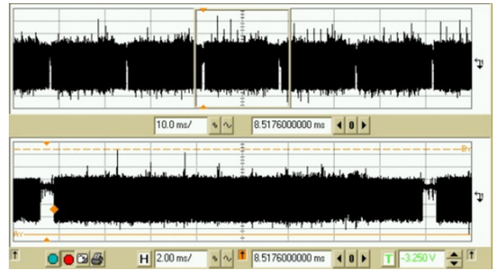
P31 LVDS (Pin 28) 10Msec / 715.7mV
Note: Pin 29 is Same but Inverted



Bottom Waveform at 2uSec

RB2_- Video Signal

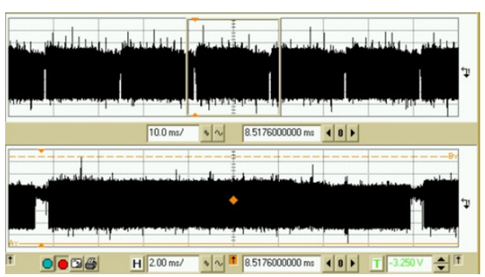
P31 LVDS (Pin 30) 10Msec / 582.8mV
Note: Pin 31 is Same but Inverted



Bottom Waveform at 2uSec

RC2_- Video Signal

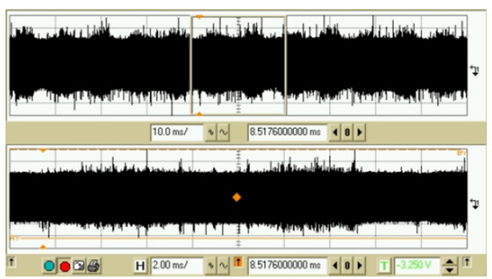
P31 LVDS (Pin 32) 10Msec / 695mV
Note: Pin 33 is Same but Inverted



Bottom Waveform at 2uSec

CLK2_- Clock Signal

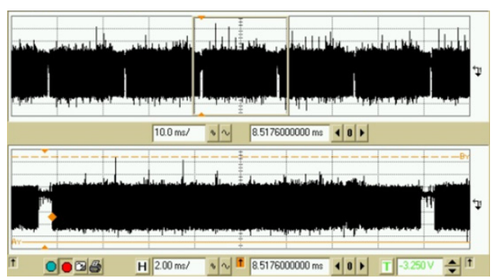
P31 LVDS (Pin 35) 10Msec / 716.5mV
Note: Pin 36 is Same but Inverted



Bottom Waveform at 2uSec

RD2_- Video Signal

P31 LVDS (Pin 38) 10Msec / 778.2mV
Note: Pin 39 is Same but Inverted



Bottom Waveform at 2uSec

The reset of the waveforms look very similar to the ones shown.

NOTE: LVDS P31 Information
There are actually 40 pins carrying Video.
8 pins are carrying clock signals to the Control board.

WAVEFORMS:
Waveforms taken using 1080P SMTP Color Bar input. All readings give their Time Base related to scope settings.

50PV450 Main Board (Front Side) Component Voltages

IC203 Winbond Serial Flash

Pin	
[1]	3.3V
[2]	3.3V
[3]	n/c
[4]	n/c
[5]	n/c
[6]	n/c
[7]	0.08V
[8]	3.3V
[9]	0V
[10]	Gnd
[11]	n/c
[12]	n/c
[13]	n/c
[14]	n/c
[15]	0.08V
[16]	0.08V

IC308 +1.3V_VDDC Regulator

Pin	
[1]	0.8V*
[2]	0V
[3]	5V
[4]	6.1V
[5]	5V
[6]	1.3V
[7]	1.3V
[8]	4.5V

*Caused Video to Mute

Q402 Tuner CVBS Buffer (Analog)

Pin	
[B]	1.1V
[E]	1.7V
[C]	Gnd

Q404 Tuner SIF Buffer (Digital)

Pin	
[B]	1.2V
[E]	1.8V
[C]	Gnd

Q502 HDMI CEC Buffer

Pin	
[1 B]	Gnd
[2 S]	3.18V
[3 D]	3.29V
[4 G]	3.3V

D1 Reset Speed Up

Pin	
[A1]	Gnd
[A]	0V
[A2]	Gnd

D2 LED-R Routing

Pin	
[A1]	0V
[C]	0.13V
[A2]	0.28V

D501 B+ Routing to IC502

Pin	
[A1]	5.1V
[A]	4.55V
[A2]	0V

D504 B+ Routing to IC503

Pin	
[A1]	5.1V
[A]	4.55V
[A2]	0V

D505 B+ Routing to IC504

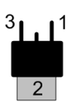
Pin	
[A1]	0V
[A]	4.54V
[A2]	5.0V

50PV450 Main Board (Back Side) Component Voltages

IC202 NVRAM

Pin	
[1]	Gnd
[2]	Gnd
[3]	Gnd
[4]	Gnd
[5]	3.3V
[6]	3.3V
[7]	Gnd
[8]	3.3V

IC301 1.8V_MST Regulator



Pin	
[1]	0.6V
[2]	1.8V (Out)
[3]	3.3V (In)

IC302 3.3V_VST Regulator

Pin	
[1]	Gnd
[2]	3.3V (Out)
[3]	5.09V (In)

IC303 3.3V_MST Regulator

Pin	
[1]	Gnd
[2]	3.3V (Out)
[3]	5.04V (In)

IC304 1.2V_DVDD Reg Dig Ch Only

Pin	
[1]	Gnd
[2]	1.2V (Out)
[3]	3.3V (In)

IC305 3.3V_TU Regulator

Pin	
[1]	2.1V
[2]	3.3V (Out)
[3]	5.1V (In)

IC307 1.8V_TU Regulator

Pin	
[1]	Gnd
[2]	1.8V (Out)
[3]	3.3V (In)

IC501 HDCP Data EEPROM

Pin	
[1]	Gnd
[2]	Gnd
[3]	3.3V
[4]	Gnd
[5]	3.3V
[6]	3.3V
[7]	3.3V
[8]	3.3V

IC502 **IC503, IC504** EDID Data For HDMI

Pin	
[1]	Gnd
[2]	Gnd
[3]	Gnd
[4]	Gnd
[5]	3.3V
[6]	3.3V
[7]	3.3V
[8]	3.3V

IC602 RGB Earphone Amp

Pin	
[1]	Gnd
[2]	Gnd
[3]	Gnd
[4]	Gnd
[5]	5.09V
[6]	5.09V
[7]	0V
[8]	5.09V

IC703 RS232 Tx/Rx

Pin	
[1]	3.3V
[2]	5.6V
[3]	0V
[4]	0V
[5]	(-5.5V)
[6]	(-5.5V)
[7]	(-5.5V)
[8]	0V
[9]	3.3V
[10]	3.3V
[11]	n/c
[12]	n/c
[13]	0V
[14]	5.6V
[15]	Gnd
[16]	3.3V (B+)

IC704 USB 5V Limiter

Pin	
[1]	Gnd
[2]	5.1V (In)
[3]	5.1V (In)
[4]	3.3V
[5]	0V
[6]	5.1V (Out)
[7]	5.1V (Out)
[8]	n/c

Q301 Driver for 5V_MST Switch Q302

Pin	
[B]	0.6V
[C]	0V
[E]	Gnd

Q302 5V_MST Switch

Pin	
[G]	0V
[S]	5.09V
[D]	5V

Q303 3.3V_PVSB Dig Ch Only

Pin	
[G]	0V
[S]	3.3V
[D]	3.3V

Only on with Dig Channel

Q304 urns on 3.3V_PVSB Switch Q303

Pin	
[B]	0.64V
[C]	0V
[E]	Gnd

Only on with Dig Channel

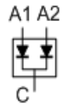
Q501, Q503
Q504 Hot Swap Switch for HDMI

Pin	
[B]	0V
[C]	0V
[E]	Gnd

Q702 RS232 Tx Buffer

Pin	
[B]	0.6V
[C]	0V
[E]	Gnd

D502 HDMI CEC Limiter



Pin	
[A1]	0V
[A2]	3.28V
[C]	3.28V

This concludes the Presentation

Thank You